CONTROL DATA® 6600
COMPUTER SYSTEM

6601 A-J, 6613-A/B/C
6604-A/B/C, 6614-A/B/C
Peripheral and Control Processor
Central Memory
Clock
Extended Core Storage Coupler
(Std Opt 10102 and/or Spec Opt 60080)
Power Wiring

Volume 2

DIAGRAMS & CIRCUIT DESCRIPTIONS

CONTROL DATA CORPORATION CUSTOMER ENGINEERING MANUAL

RECORD of REVISIONS

REVISION	NOTES
A	Equation Lists and Appendix A added. Miscellaneous changes made for purposes of clarification.
B	Central Memory diagrams added, sheets 38-44. Central Processor diagrams added, sheets
	45-114. Clock diagrams added, sheets 115-121. Corrections made to Appendix A.
C	This reprint obsoletes all previous editions. Central Processor completely revised.
(3-29-65)	Miscellaneous changes made for purposes of clarification. This printing includes Change Order
	10946.
D	Volumes 1 and 2 obsolete all previous editions. "Add Unit" diagrams added in Volume 1.
(7-12-65)	Miscellaneous changes made for purposes of clarification. This printing includes Change Order
	11826.
E	Change Order 12006.
F	Change Order 12051.
G	Change Order 12082.
H	Change Order 12182.
J	Change Order 12187.
K	Publication Change Order 12481. The following pages have been revised: 6601/04 Central
(1-27-66)	Processor - 1, 3, 4.1, 4.2, 5, 7, 9, 13, 15, 16, 19, 21, 23, 24.1, 25, 29, 31, 33, 35, 43, 53,
	57, 61, 63, 64, 65, 66, 67, 68.0, 68.1, 68.3, 68.5, 68.7, 68.9, 69, 70, 71, 73, 74, 74.1, 75,
	77, 79, 80.1, 80.3, 81, 82, 83, 85, 86.1, 86.3, 87, 88.1, 89, 91, 99, 101 and 103. 6601/04
	Functional Units - Contents, 2.3, 3, 5, 7, 9, 11, 13, 14.1, 14.3, 14.4, 14.5, 14.7, 14.8, 15,
	16, 17, 19, 23, 25, 26, 29, 31, 33, 35, 37, 43, 44, 47, 48, 49, 51, 53, 55, 57, 59, 61, 63, 64,
	67, 95, 97, 103, 126.1, 126.2, 127, 181, 182.0, 183, 185, 187, 189, 190, 191, 193, 194, 197,
	201, 205, 207, 211, 213 and Comment Sheet. 6601/04 Peripheral and Control Processor - 1, 2,
	3, 5, 9, 11, 19, 21, 39, 47, 55, 57, 58, 59, 61, 63, 65 and 67. 6601 Central Memory (131K) -
	Contents, 1, 3, 5, 11, 12.0, 12.1, 12.2, 13, 14.0, 14.1, 14.3, 15. 6604 Central Memory (65K)
	Contents, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14.1, 15. 6601/04 Clock - 3, 5, 7, 9, 11,
	13, 15, 17. 6601/04 Power Wiring - Contents, 1, 3, 5, 6, 7, 9, 11, 12, 13, 15, 17. 6601/04
	Appendix A - Title page, 2 and Comment Sheet.
L	Field Change Order 13358 which advanced the Product Designation to 6601-H31, 6604-A33 and
(6-28-66)	6605-A12. Central Processor pages 11, 13, 17, 19, 22.1, 24.01, 24.1, 25, 37, 41, 45, 86.01
	and 90.1 revised. Functional Units pages 5, 11, 14.21, 14.3, 14.5, 182 and 185 revised.
M	Publications Change Order 13629 which incorporated Change Orders 11310, 11389, 11467, 11487,
(6-28-66)	11826, 11937, 12006, 12450, 12543, 12655, 12656 and 12761 into this Manual. Vol. 1 Pages
	changed: Cover, Title page, Record of Revisions, Key to Logic Symbols, Central Processor
	Contents, 7, 19, 21, 22.1, 23, 24.01, 24.1, 35, 36.1, 39, 40.1, 43, 44.1, 63, 79, 80.01, 80.3,
	81, 82.1, 85, 86.01, 86.1, 86.3, 87, 88.1, 89, 90.1, 91, 101, 103 and 105. Functional Unit
	Contents, 3, 5, 7, 9, 11, 13, 14.1, 14.21, 14.3, 14.5, 14.7, 15, 39, 63, 99, 101, 103, 137,
	149, 173, 181, 182.01, 182.1, 185, 187, 197 and 213. Vol. 2 Pages changed: Cover, Title page, Record
	of Revisions, Key to Logic Symbols, Peripheral Processor Contents, 5, 6.1 and 6.2. Central
	Memory (131K) Contents, 10.1 and 11. Central Memory (65K) Contents, 11 and 12.1.

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or use Comment Sheet in the back of this manual.

RECORD of REVISIONS (CONT'D)

REVISION	NOTES
M (Con't)	Clock Contents 1, 3, 4.1, 11, 12.1.
N thru AP	Publication Change Order 14798 which incoporated the following Change Orders: 13415, 13512,
(10-10-66)	13513, 12930, 13536, 13545, 13569, 12932, 12933, 12931, 13731, 13814, 14136, 13999, 14045,
	14111, 14112, 14153, 13757, 14202, 14203, 13746 and 13756. Vol. 1 Pages changed: Central
	Processor 23, 24.01, 24.1, 31, 55, 71, 86.01, 86.3, 87, 89 and 90.1. Functional Units 19, 31,
	61, 63, 73, 93, 125, 157, 161, 175, 197, 209, 211 and 213. Vol. 2 Peripheral and Control
	Processor page 67. 6601/6613 Central Memory (131K) page 7. 6604/6614 Central Memory
	(65K) pages 7 and 12.1. 6601/6604/6613/6614 Clock page 15 and 17.
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(3-22-67)	15218, 15252, 15338, 15339, 15191, 15562, 15563, 15068 and 15750. Vol. 1 pages changed:
	Central Processor 31, 39, 81, 82.1, 89, 99 and 105. Functional Units 101. Vol. 2 pages
	changed: Peripheral and Control Processor 5, 15 and 23. Clock - Contents and page 3. Power
	Wiring - Pages 7, 9, 13 and 15 revised. Pages 19, 21, 23 and 25 added. Cover and title page
	revised for Vol. 1 and Vol. 2.
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(11-9-67)	15829, 15968, 15985 and 16269. Vol. 1 pages changed: General Contents (new). Central
	Processor 17 and 91. Functional Units 3, 14.5, 31, 93, 101, 103, 107, 117, 123, 163, 173,
	181, 182.0, 187, 189, 203 and 213. Vol. 2 pages changed: Cover and Title Page, General
	Contents (new), Peripheral and Control Processors 3, 5, 25, 29, 49, 53, 55 and 57. Central
	Memory (131K) 8.1. Central Memory (65K) 8.1. Clock, page 3. E.C.S. Coupler Section
	Pages 1 thru 37 (new). Power Wiring 1, 19, 21, 23 and 25.
BM thru BT	Publication Change Order 18437, which incorporated the following Change Orders: 17014, 17269,
(1-12-68)	17251, 17346 and 17660. Vol. 1 pages changed: Central Processor, pages 7, 9, 11, 13, 19, 22.1,
	24.01, 41, 67, 68.7, 69, 71, 87, 90.1, 91 and 105; Functional Units pages 3, 5, 7, 9, 11, 14.1, 14.3, 14.5,
	14.7, 19, 31, 61, 63, 75, 77, 79, 81, 83, 85, 93, 95, 97, 101, 103, 105, 109, 111, 117, 119, 121, 123, 125, 133,
	135, 137, 139, 141, 145, 147, 149, 151, 153, 155, 159, 161, 163, 165, 167, 169, 173, 175, 180.3, 180.7, 185, 197,
	199, 207, 209, 211 and 213. Vol. 2 pages changed: Peripheral and Control Processors pages 6.1, 7, 9,
	19, 21, 25, 29, 31, 37, 39, 41, 47, 51, 55, 57, 59, 61, 65, and 67; Central Memory (131K) pages 4, 5, 8, 8.1,
	11 and 15. Central Memory (65K) pages 4, 5, 8 and 15. Clock Section pages Clock Contents, 4.1,
	5, 7.1, 7.3 (new), 9.1, 9.3 (new), 12.1, 12.3 (new), 13, 15 and 17. Appendix pages 12 and 14.

FORM CA 230-2

GENERAL CONTENTS

FOREWORD

Logic diagrams contained in this manual do not attempt to show the entire device, nor even depict complete modules within that device. The purpose of the diagrams is to show the logical significance of circuits that may involve parts of many modules on several chassis. Logic hardware that is not pertinent to the particular logic sequence being illustrated is not included. Certain areas may not be shown at all, while others may appear on several drawings. These limitations are important to remember; the logic diagrams do not replace the 6000 Series chassis and cable tabs, but they are a valuable tool in understanding the tabs and the overall operation of the machine.

KEY TO LOGIC SYMBOLS

(Standard 6000 Series Card Types)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA* logic, two signals, a logical "0" and a logical "1" are the possible input or output conditions of a circuit. For example, "1" is considered "up" and "0" is considered "down" on a timing chart. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 6000 Series card types are inverters, test points, flip-flops, twisted pair line drivers, and coaxial cable line drivers.

Inverters

An inverter is a logic element which provides an output that is a negation of its input. When more than one input is provided to an inverter, "0's" take precedence over "1's" and therefore drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. The basic inverter is shown in the logic diagrams as an arrow into either a circle or a square (Figure 1). Both symbols represent the same electronic circuit and have the same logic interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain.

Figure 1. Inverter Symbols

Certain card types employ variations of the standard inverter building block. These differences are indicated in the logic diagrams by a dot or a cross in the circle or square (Figure 2). Both the chassis tabs containing the card in question and the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700) contain electronic schematics of these special variations.

*Registered trademark of Control Data Corporation

Figure 2. Special Inverters

Acceptable conventions for showing multiple inputs and outputs are given in Figure 3. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.

Figure 3. Multiple Inputs/Outputs

Acceptable conventions for showing inverter networks are illustrated in Figure 4. As a general rule, circle inverters alternate with square inverters wherever possible. Because multiple outputs are identical, only one arrow is shown in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D; in this case because B is not the only input to C or D).

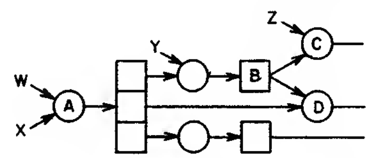


Figure 4. Inverter Networks

Test Points

A test point has no logic function, but is shown in the logic diagrams as a triangle (Figure 5). They are numbered from 1 to 6.

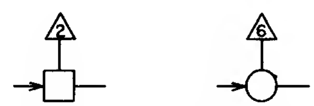


Figure 5. Test Point Symbols

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states--designated as Set and Clear--and is composed of two inverters (Figure 6). The flip-flop is said to be set when the set output (B) is a "1", and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop and (C) must be "0" to clear it.

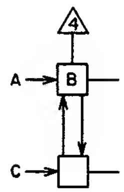


Figure 6. Flip-Flop Symbol

Logic signals are transmitted from one module to another by means of a line driver. Modules on the same chassis are connected with twisted pair lines, and those on separate chassis are connected by coaxial cable.

Twisted Pair Drivers

The twisted pair driver is represented by the standard square or circle. The output of the square or circle, however, is connected to a pin of the module in question and wired from there to a pin on another module (Figure 7). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28 (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams). The module location is shown above the card, and the module type is denoted in the upper right corner.

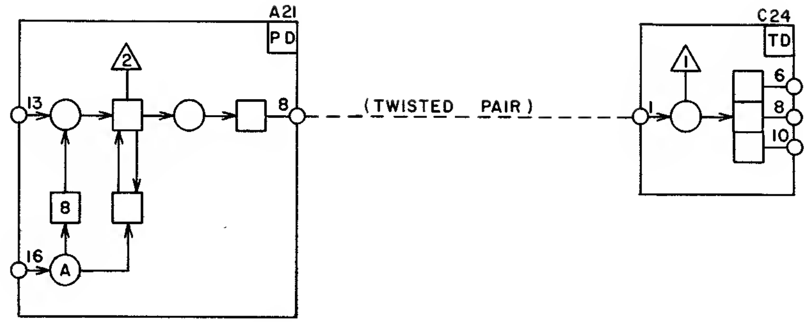


Figure 7. Twisted Pair Line Driver

Coaxial Cable Drivers

The coaxial cable driver is a 25 nsec pulse circuit, and is represented as shown in Figure 8. The pins used are represented by a small double circle.

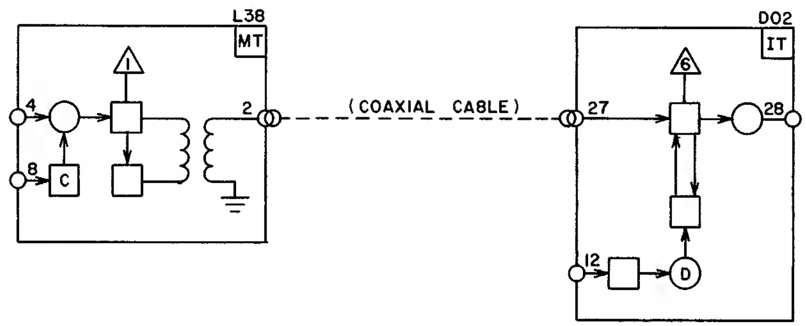


Figure 8. Coaxial Cable Driver

PERIPHERAL AND CONTROL PROCESSORS

CONTENTS

PERIPHERAL AND CONTROL PROCESSORS

INTRODUCTION

The CONTROL DATA 6601 Central Computer consists of ten peripheral and control processors, a central processor, central memory, and peripheral equipment controllers. Each peripheral and control processor is an independent computer with 4096 words of core storage and a repertoire of 64 instructions. The peripheral and control processors share access to central memory and to 12 bi-directional input-output channels.

The ten peripheral and control processors are combined in a multiplexing arrangement which allows them to share common hardware for arithmetic, logical, I/O, and other operations without sacrificing speed or independence. This multiplexing arrangement consists of the barrel, the slot, and common paths to storage and I/O channels.

The barrel is a matrix of FFs used to hold the quantities in the operating registers of the ten processors and to give each a turn to use the execution hardware in the slot (adders, shift network, etc.). The quantities in the barrel are shifted from slot output to slot input. Each time a processor's data enters the slot, a portion of the instruction is executed. A trip around the barrel requires 1000 nsec (one major cycle), of which each processor's data spends 900 nsec in the barrel and 100 nsec in the slot. Each processor has its own independent 4096 word memory which may be referenced once each major cycle (once each trip around the barrel).

The peripheral and control processors read data from input devices, perform preliminary arithmetic and logical operations, send data and programs to central memory, assign tasks to the central processor, read central processor results from central memory, and send results to external storage (magnetic tape, disc file, etc.) or to output devices (line printer, display console, etc.).

Characteristics of the peripheral and control processors are:

-- 4096 word magnetic core storage (12-bits)
   Random access, coincident current
   Major cycle - 1000 ns
   Minor cycle - 100 ns

-- 12 bi-directional input-output channels
   All channels available to all processors
   Maximum transfer rate per channel - one word/major cycle.

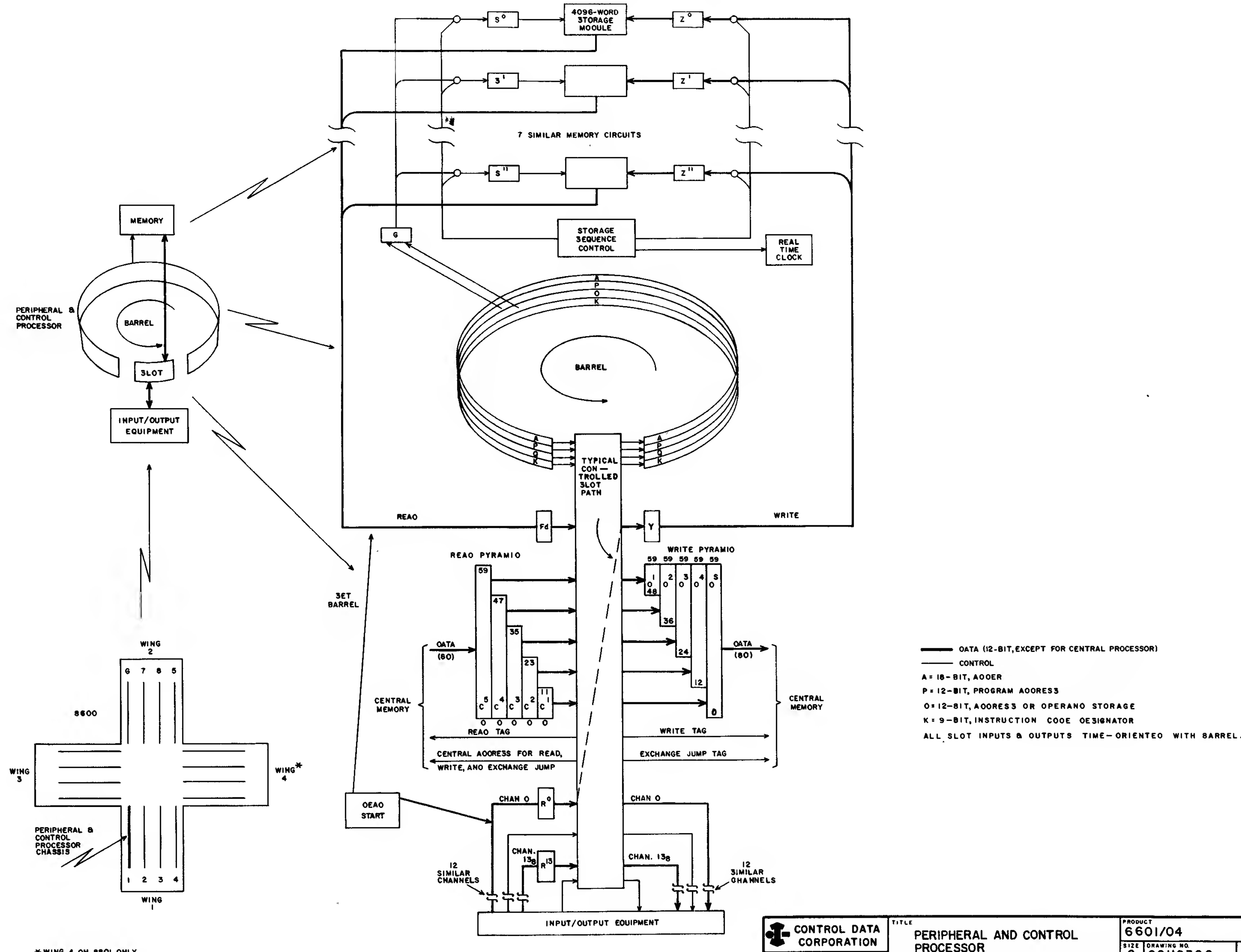
-- Real-time clock (period 4096 major cycles)

-- Instructions
   Arithmetic
   Logical
   Input-output
   Central memory read/write
   Exchange jump

-- Average instruction execution time - two major cycles

-- Indirect addressing

-- Indexed addressing



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR OVER-ALL BLOCK DIAGRAM

PRODUCT: 6601/04
SIZE: C | DRAWING NO. 60119300 | REV
SHEET 3 | 1

EQUATION LISTS

P Register and P Incrementer

P Incr. → $P = \overline{Q \rightarrow P}$

Q Adder → P=011+022+(64X. active)+(65X. inactive)+(66X. full)+(67X. empty)+(03+(04. A=0)+(05. A=$\overline{0}$)+(06. A pos)+(07. A neg)). (K=00X)

Adv. P = (K=00X). ($\overline{26+60}$)+5X5+(26. central $\overline{\text{busy}}$. K=00X)+021+5XX+2XX+64X+65X+66X+67X+713+733+(637. central $\overline{\text{busy}}$)+(617. Q≠0. central $\overline{\text{busy}}$. $\overline{C}^5$)+613. $\overline{C}^4$. C^5+614. $\overline{C}^3$+615. $\overline{C}^2$+616. $\overline{C}^1$+633. $\overline{D}^1$+634. $\overline{D}^2$+635. $\overline{D}^3$+636. $\overline{D}^4$+712. full +(732. empty. active)+(77X inactive)+central $\overline{\text{busy}}$. $\overline{C}^5$. ($\overline{C}^1$+$\overline{C}^2$+$\overline{C}^3$+$\overline{C}^4$). (K=00X). (F=60)

Fd → P = 612. central $\overline{\text{busy}}$. $\overline{C}^5$. ($\overline{C}^1$+$\overline{C}^2$+$\overline{C}^3$+$\overline{C}^4$)+632+711+731+733+713

Zero → P = dead start. (clock= 7777)

A Register and A Adder

10000_8 → A = dead start. (clock=7777)

X → A = 27 (K=00X)

Fd → A = 37X+471+572+36X+461+562

A → A = $\overline{\text{14X+15X+20X+27X+30X+36X+37X+401+461+471+502+562+572+70X}}$

R → A = 70X

+1 → B_L = 36X+461+562+(637. central $\overline{\text{busy}}$)+614. $\overline{C}^3$

-1 → B_L = 712 . full+ 37X+471+572+(732. active. empty)

+d → B_L = 10+12+14+16+20X+21X+22X+31X+35X+411+451+552+30X+401+502

-d → B_L = 11+13+15+17+23X+33X+431+532+32X+421+522

+F → B_M = 20X+21X+22X+30X+31X+35X+401+411+451+502+512+552

-F → B_M = 23X+33X+431+532+32X+421+522

00 → B_M = 10+12+14+16+36X+461+562+(614. $\overline{C}^3$)+(637. central $\overline{\text{busy}}$)

00 → B_U = 30X+31X+35X+36X+401+411+451+461+502+512+552+562+10+12+14+16+(614. $\overline{C}^3$)+(637. central $\overline{\text{busy}}$)

+Q_L → B_U = 20X+21X+22X

-Q_L → B_L = 23X

Q Adder Controls

Q_L → Q Adder = $\overline{\text{010+020+4X0+5X0+630+64X+65X+66X+67X+610+K=00X}}$

P → Q Adder = (03 +04 +05. +06 +07) (K=00X)

+1 → H_L. H_U = 022+(60X. C^5. $\overline{C}^4$ K=XX0)+(601. $\overline{C}^3$)+602. $\overline{C}^2$+603. $\overline{C}^1$+620. $\overline{D}^1$+621 $\overline{D}^2$+622. $\overline{D}^3$+623. $\overline{D}^4$

d → H_L = 00X+010+020+021+011+4X0+5X0+5X1+2XX+64X+65X+66X+67X+610+630

F → H_U = 011+021+5X1+2XX+010+020+610+630+64X+65X+66X+67X+4X0+5X0

-1 → H_L = 615. $\overline{C}^2$+635. $\overline{D}^3$

+00 → H_U = $\overline{\text{((03+04+05+06+07). }d^5\text{)}}$(K=00X)

G Register

P → G = $\overline{\text{(Q → G)+(713+733+710+730+611+631)}}$

Q → G = 010+020+022+4XX+610+630+60X+62X+3X0+5X0+5X2

K Register

K → K = $\overline{\text{2XX+(70X. clock select)+(70X. full)+(72X. active. empty)+(74X inactive)+(75X. active)+(76X. inactive)+3XX+4X1+5X2+011+022+64X+65X+66X+67X+713+733+604+(624) (central }\overline{\text{busy}}\text{)+(77X}}$ inactive)

340 → K = 35X+36X+37X+451+461+471+552+562+572

F → K = 01+02+20+21+22+23+3X+4X+5X+(F^5. $\overline{60}$)+(60. central $\overline{\text{busy}}$ $\overline{C}^5$ ($\overline{C}^1$+$\overline{C}^2$+$\overline{C}^3$+$\overline{C}^4$))

712 → K = load. dead start (clock=7777)

732 → K = dump. dead start. (clock=7777)

505 → K = sweep. dead start. (clock= 7777)

Adv K = 010+020+610+630+ 021+5X1+4X0+5X0+632+711+731+((712+732). inactive)+611+631+710+730+((01+02+5X). d=0. K=00X)+(600. C^5 $\overline{C}^4$)+(601 $\overline{C}^3$)+(602. $\overline{C}^2$)+(603. $\overline{C}^1$)+(613. $\overline{C}^4$ C^5)+(614 $\overline{C}^3$). (615. $\overline{C}^2$)+(616. $\overline{C}^1$)+(620. $\overline{D}^1$)+(621 $\overline{D}^2$)+(622. $\overline{D}^3$)+(623. $\overline{D}^4$)+(633. $\overline{D}^1$)+(634. $\overline{D}^2$)+(635. $\overline{D}^3$)+(636. $\overline{D}^4$)+(712 full. A=1)+(732 empty. A=1)+(612. central $\overline{\text{busy}}$ $\overline{C}^5$ ($\overline{C}^1$+$\overline{C}^2$+$\overline{C}^3$+$\overline{C}^4$))

Clr K^2 = 617. Q=0+617. central $\overline{\text{busy}}$ $\overline{C}^5$. Q=$\overline{0}$+637. central $\overline{\text{busy}}$

Set K^6 = 617. Q=0+637. central $\overline{\text{busy}}$ Q=0

A Adder Control

Add = $\overline{\text{10+11+12+13+22X+23X+33X+431+532}}$

Selective = 11+12+13+22X+23X+33X+431+532

Logical Prod. = 12+13+22X

Shift = 10

Q Register and Q Adder

000 000 00X XXX → Q = dead start (clock=7777)

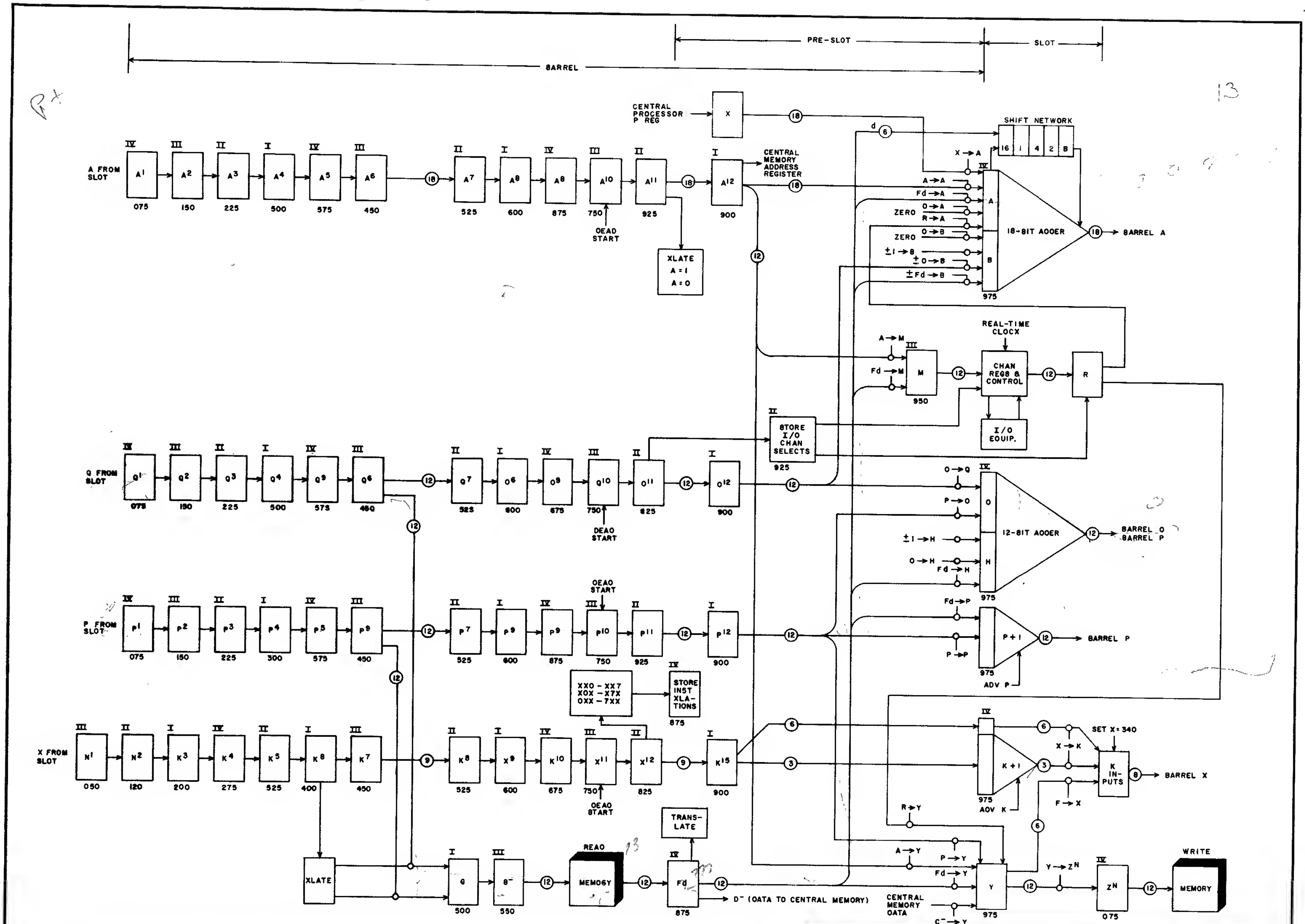
1 → Q^1 = dead start (clock=7777) Minor cycle 8+9+4+5

1 → Q^2 = dead start (clock=7777) Minor cycle 6+7+8+9

1 → Q^3 = dead start (clock= 7777) Minor cycle 0+1

1 → Q^0 = dead start (clock=7777) Minor cycle 1+3+5+7+9

Q Adder → Q = Unconditional

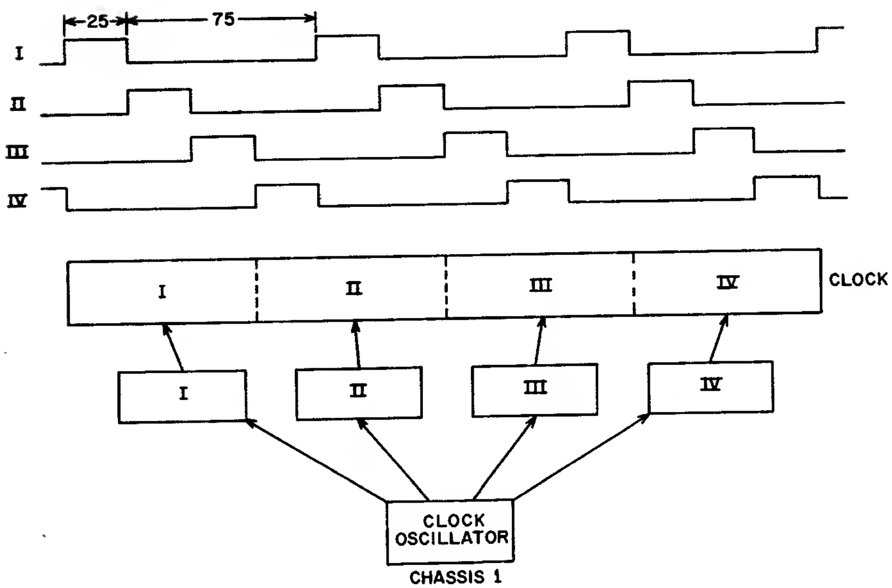


NOTE
ALL PERIPHERAL AND CONTROL PROCESSOR MODULES ON CHASSIS 1
THIS SHEET IS IDENTICAL TO APPENDIX A PAGE 2.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR DETAIL BLOCK DIAGRAM	PRODUCT 6601/04 SIZE C DRAWING NO. 60119300 REV SHEET 4 3

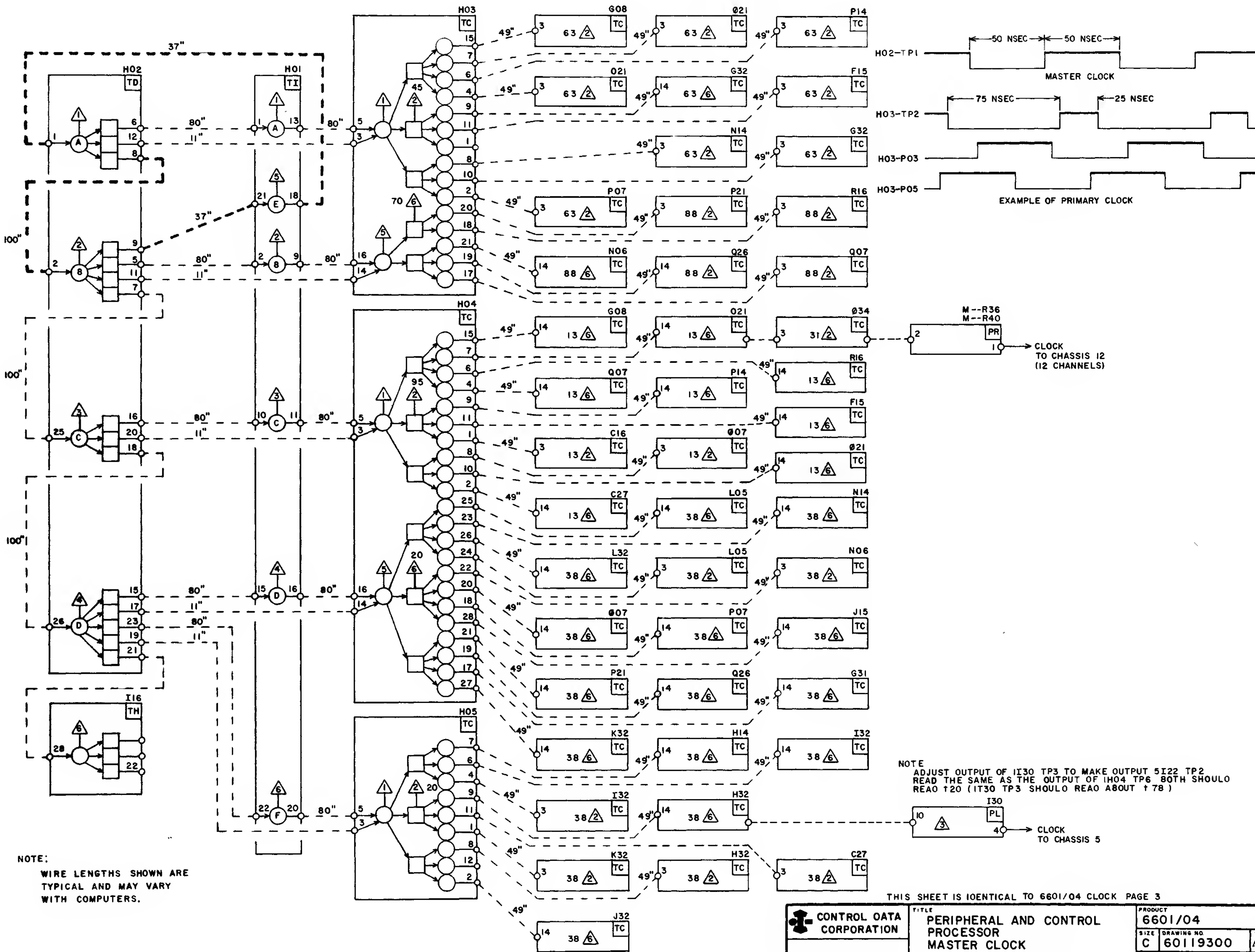
TIMING

Timing in the 6600 is controlled by a four-phase master clock located on the peripheral and control processor chassis (chassis 1). Four 25 nsec pulses are issued each minor cycle to control movement of data and instructions. A storage sequence control system, timed by the four-phase clock, controls storage references and defines the ten peripheral and control processors.



MASTER CLOCK

The master clock oscillator consists of a TD module and a TI module. To form the 25 usec clock pulses, a pulse from the TD is ANDed with a similar pulse which has been delayed and inverted by the TI. The result is a series of pulses (primary clock) which are fanned out through TC modules to be used as timing control. In addition to forming the clock pulses on chassis 1, the master clock sends pulses to chassis 5 and from there to all the other chassis. On each chassis, the incoming clock pulses are used to form a clock system similar to chassis 1. The clocks on all chassis are synchronized so that time 00 on any chassis is the same as time 00 on any other chassis.

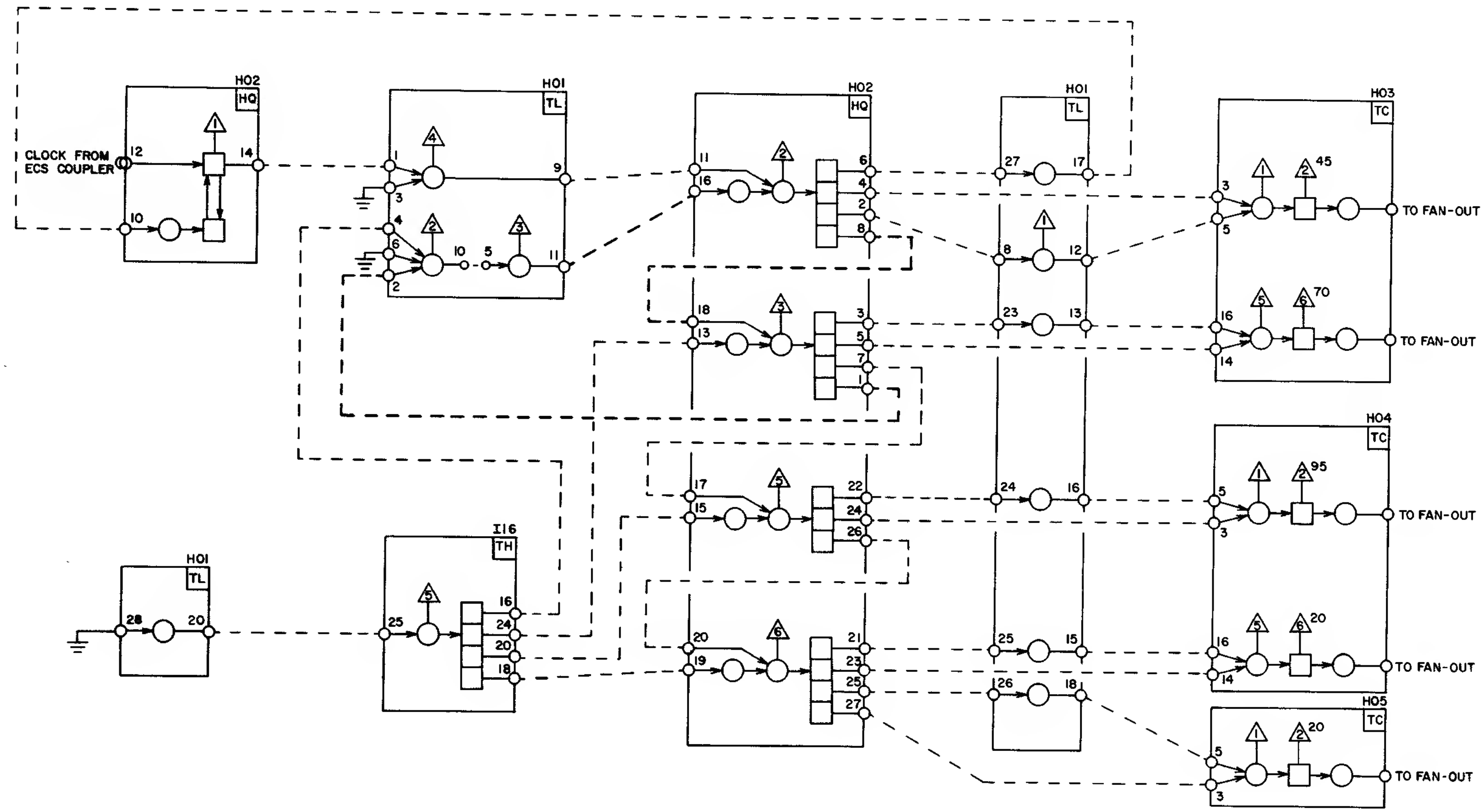


NOTE
ADJUST OUTPUT OF 1I30 TP3 TO MAKE OUTPUT 5I22 TP2 READ THE SAME AS THE OUTPUT OF 1H04 TP6 BOTH SHOULD READ ↑20 (1I30 TP3 SHOULD READ ABOUT ↑78)

NOTE:
WIRE LENGTHS SHOWN ARE TYPICAL AND MAY VARY WITH COMPUTERS.

THIS SHEET IS IDENTICAL TO 6601/04 CLOCK PAGE 3

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR MASTER CLOCK CHASSIS 1 SERIALS 1-7	PRODUCT 6601/04 SIZE C DRAWING NO. 60119300 REV F SHEET 268



NOTES:

1. TURN TO PAGE 5 FOR COMPLETE CLOCK FAN-OUT ON CHASSIS 1.

THIS SHEET IS IDENTICAL TO 6601/04/13/14 CENTRAL PROCESSOR CLOCK, P. 4 1

CONTROL DATA CORPORATION	TITLE: PERIPHERAL AND CONTROL PROCESSOR MASTER CLOCK CHASSIS 1, SERIALS 8-UP	PRODUCT: 6601/04/13/14	
COMPUTER DIVISION		SIZE: C · DRAWING NO.: 60119300	REV: BT
		SHEET: 266	6.1

BARREL

The barrel contains the A, P, Q, and K registers for each of the ten processors. The functions of these four registers in the barrel are:

A (18 bits) A holds one operand for add, shift, logical and selective operations. The 18-bit quantity in A may be an arithmetic operand, central memory address, or an I/O function or data word.

P (12 bits) P is the program address register. (P) is also used as a data address in certain I/O and central instructions.

Q (12 bits) Q holds the d portion of instructions or may hold a data word when d is an address.

K (9 bits) K holds the F portion of an instruction word and the trip count (the number of times an instruction has been around the barrel).

A REGISTER

The A register in the barrel receives the result of add, shift, logical or selective operations in the slot. This quantity may be stored, returned to the slot unaltered or used to condition other operations. A is always tested to determine its sign and whether it is zero, non-zero, or one. The result of these tests may be used to condition jump or other instructions. The quantity in A may be a full 18-bit central address or a 12-bit peripheral word (in which case the upper 6 bits will be zero).

The connections to A in the barrel are:

Outputs

A → M - (A) may be sent as a data or function word on one of the I/O channels.

A → Central Address Register - (A) is the central memory address in central read and write and exchange jump instructions.

A → Y - For a store instruction, (A) is sent to Y and then to storage.

A → Translation Networks

Inputs

X → A - The content of the central program address register is sent to the peripheral X register every minor cycle. A 27 instruction sends (X) to A and enables a peripheral and control processor to monitor the progress of the central program.

R → A - An input to A instruction gates a word from an I/O channel into A.

Fd → A - A data word from storage is entered into A by the Fd → A path.

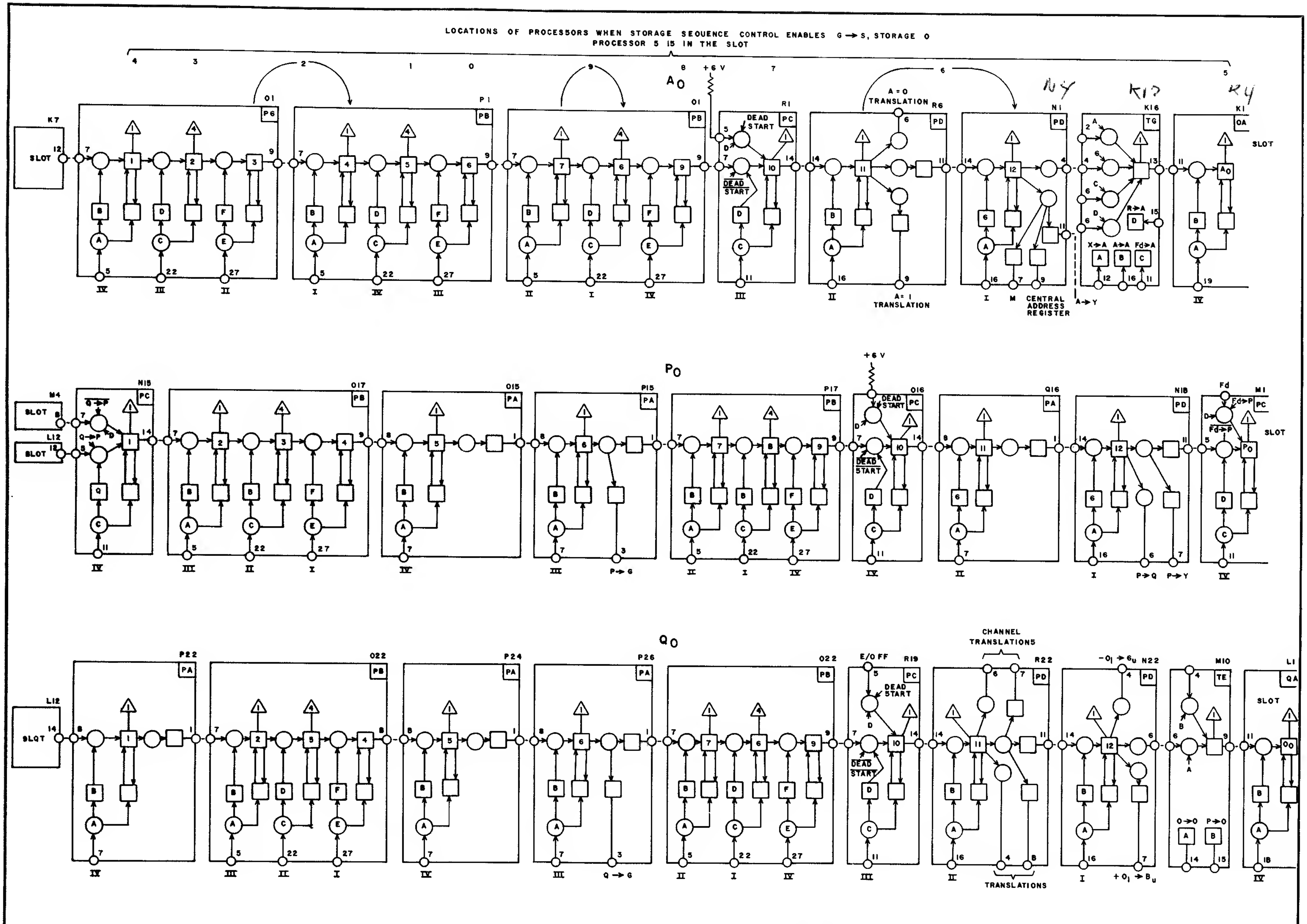
A → A - When the quantity in A is to be returned to the slot unaltered, the A → A gate is enabled.

P REGISTER

P holds the program address and is not changed in the barrel (except by Dead Start). (P) is sent to a storage unit from stage 6 in the barrel. This allows time to read a word from storage and make it available at slot time. (P) is sent to the G register which feeds all ten storage address or S registers. When a jump is called for, P is sent to Q from barrel stage 12. Q is then altered by the Q adder in the slot and the new address returned to P at the first stage of the barrel.

Q REGISTER

Q holds the d portion of an instruction and has several outputs to translation networks which make channel selections for I/O instructions. When d is an address, (Q) is sent from the slot to P in the barrel and the word obtained from that address is entered into Q in the slot. When a jump is called for, the quantity in Q is added to or subtracted from (P) in the Q adder and the result sent to P. When an instruction calls for an 18-bit operand, the lower six bits of Q are sent to the upper six bits of A to form the 18-bit quantity dm.



CONTROL DATA CORPORATION

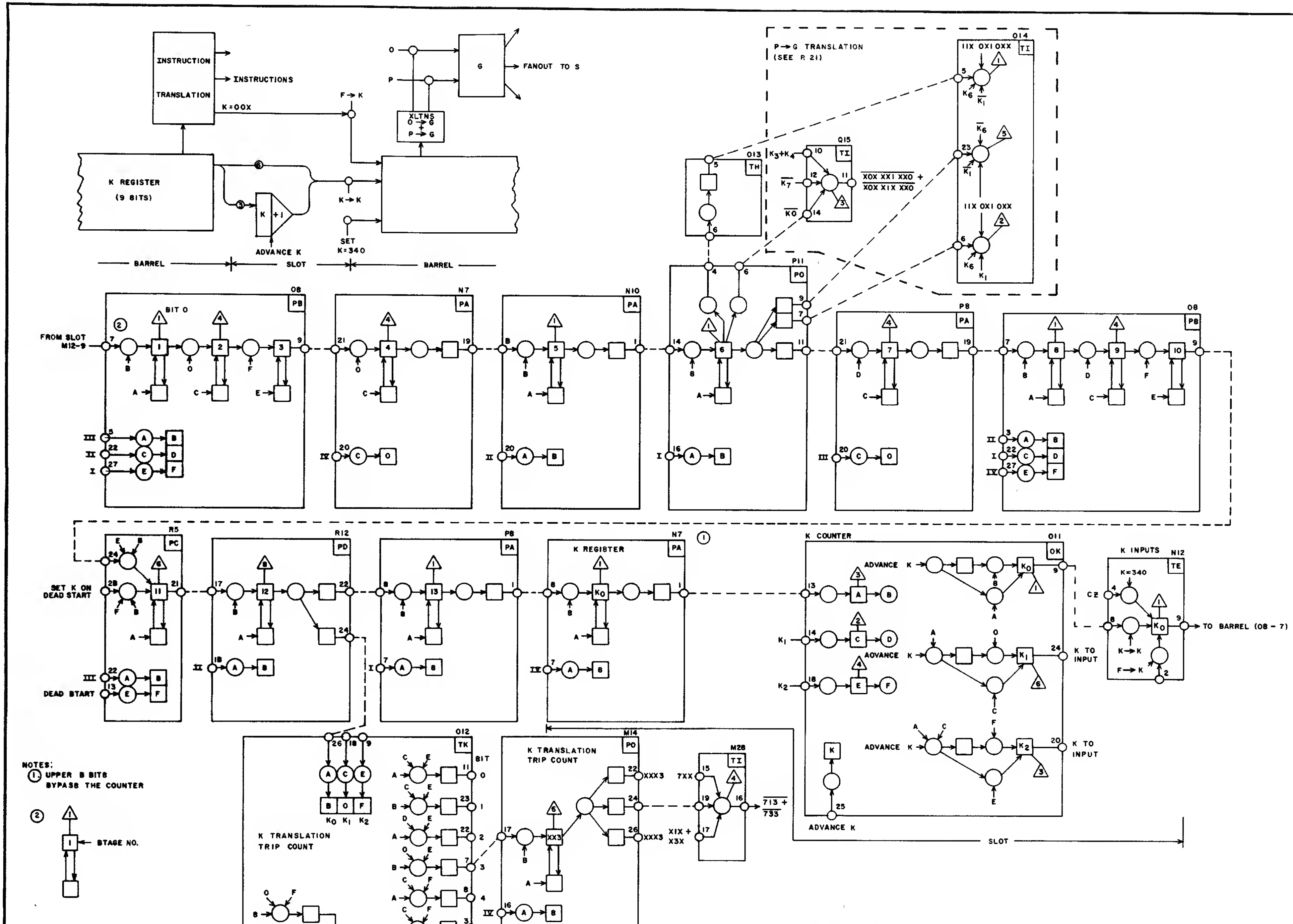
COMPUTER DIVISION

TITLE PERIPHERAL AND CONTROL PROCESSOR
A, P, Q TYPICAL BARREL PATHS

PRODUCT		
6601		
SIZE C	DRAWING NO. 60119300	REV BT
	SHEET 7	7

K REGISTER

K holds the F portion of an instruction word and a 3-bit trip count which sequences the execution of an instruction. K is translated at two different times during a trip around the barrel; first, to determine if a storage reference is needed, and second, to provide the proper commands at the slot. During the barrel trip in which a new instruction is being read from storage, a translation of K = 00X enables translations from Fd in the storage cycle path to be used in place of K translations. This eliminates the need for a separate "Read Next Instruction" trip through the barrel and allows certain instructions to be read from storage and executed all in one trip. The K = 00X translation arises from the fact that K is cleared at the end of each instruction.



NOTES:
1. UPPER 8 BITS BYPASS THE COUNTER
2. STAGE NO.

CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR K_0 BARREL AND SLOT PATHS, AND TYPICAL TRANSLATIONS

PRODUCT			
6601/04			
SIZE C	DRAWING NO. 60119300	REV BT	
	SHEET 8		9

The slot contains the execution hardware for A, P, Q, and K. Each processor is allowed one minor cycle in the slot every major cycle. Included in the slot are:

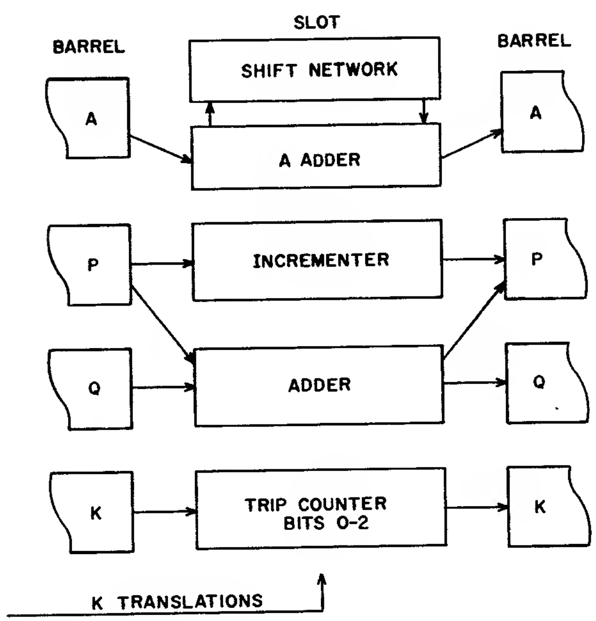
A Adder
Shift Network
Logical Circuits
Selective Circuits

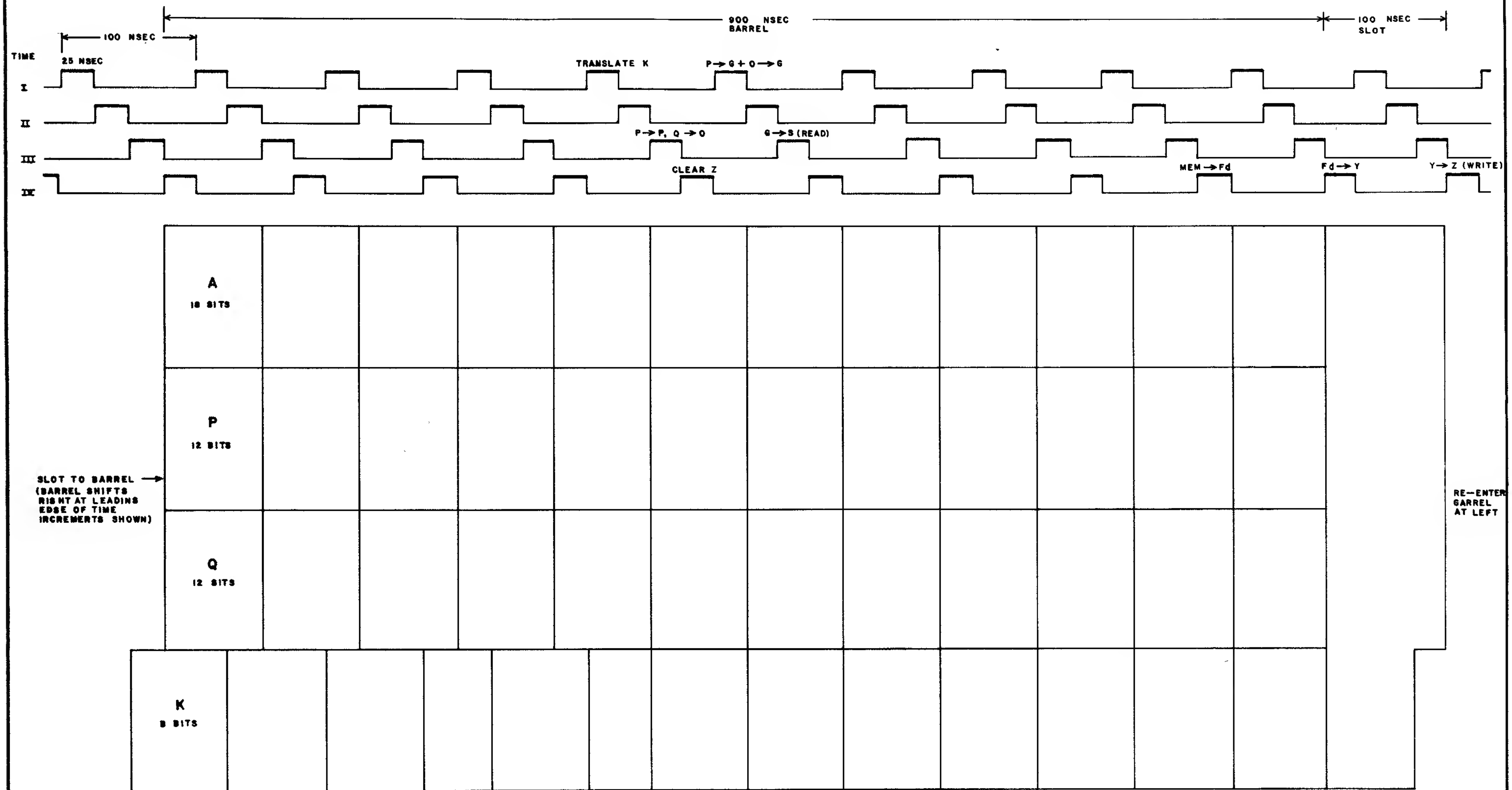
P Incrementor
Inputs from P or Q in the barrel

Q Adder
Input Path from Fd

K 3-bit Trip Counter
Input from F
K = 340 Gate

As A, P, Q, and K enter the slot, K translations (started earlier in the barrel) become available and a portion (or all) of an instruction is executed. The results are gated back into the barrel to be stored, used again, or sent to I/O equipment.





CONTROL DATA CORPORATION	TITLE PERIPHERAL AND CONTROL PROCESSOR BARREL TIMING	PRODUCT 6601/04	
COMPUTER DIVISION		SIZE C	DRAWING NO. 60119300
		REV 1	SHEET 9 / 11

	IV	III	II	I	IV	III	II	I	IV	III	II	I	GATES	IV
A0	O1 PB 1	4		P1 PB 1	4		Q1 PB 1	4		R1 PC 1	R8 PD 1	N1 PD 1	K16 TG 1	K1 DA 1
A1	2	5		2	5		2	5		2	2	2	2	2
A2	3	6		3	6		3	6		5	5	5	5	5
A3	Q2 PB 1	4		P2 PB 1	4		Q2 PB 1	4		6	6	6	6	K2 QA 1
A4	2	5		2	5		2	5		R2 PC 1	R9 PD 1	N2 PD 1	K17 TG 1	2
A5	3	6		3	6		3	6		2	2	2	2	5
A6	O3 PB 1	4		P3 PB 1	4		D3 PB 1	4		5	5	5	5	K3 QA 1
A7	2	5		2	5		2	5		6	6	6	6	2
A8	3	6		3	6		3	6		R3 PC 1	R10 PD 1	N3 PD 1	K18 TG 1	5
A9	O4 PB 1	4		P4 PB 1	4		Q4 PB 1	4		2	2	2	2	K4 QA 1
A10	2	5		2	5		2	5		5	5	5	5	2
A11	3	6		3	6		3	6		8	6	6	6	5
A12	O5 PB 1	4		P5 PB 1	4		Q5 PB 1	4		R4 PC 1	R11 PD 1	N4 PD 1	K19 TE 1	K5 DA 1
A13	2	6		2	5		2	5		2	2	2	2	2
A14	3	6		3	6		3	6		5	5	5	3	5
A15	O5 PB 1	4		P6 PB 1	4		Q6 PB 1	4		6	6	6	4	K6 QA 1
A16	2	5		2	5		2	5		R5 PC 1	R12 PD 1	N5 PD 1	5	2
A17	3	6		3	6		3	6		2	2	2	8	5

A

	IV	III	II	I	IV	III	II	I	IV	III	II	I	IV
P0	N15 PC 1	O17 PB 1	4		O15 PA 1	P15 PA 1	P17 PB 1	4		Q18 PC 1	D18 PA 1	N16 PD 1	M1 PC 1
P1	2	2	6		2	2	2	5		2	2	2	2
P2	6	3	8		3	3	3	6		5	3	5	5
P3	8	O18 PB 1	4		4	4	P18 PB 1	4		6	4	8	8
P4	N16 PC 1	2	5		5	5	2	5		Q19 PC 1	5	N19 PD 1	M2 PC 1
P5	2	3	6		6	6	3	6		2	6	2	2
P6	5	O19 PB 1	4		O16 PA 1	P16 PA 1	P19 PB 1	4		5	Q17 PA 1	5	5
P7	5	2	5		2	2	2	5		6	2	6	6
P8	N17 PC 1	3	6		3	3	3	6		Q20 PC 1	3	N20 PD 1	M3 PC 1
P9	2	O20 PB 1	4		4	4	P20 PB 1	4		2	4	2	2
P10	5	2	5		5	5	2	5		6	5	5	5
P11	6	3	6		6	6	3	6		6	8	6	8

P

LOCATION

TEST POINT

C4 PB 3

MODULE TYPE

	IV	III	II	I	IV	III	II	I	IV	III	II	I	GATES	IV
Q0	P22 PA 1	O22 PB 1	4		P24 PA 1	P25 PA 1	Q22 PB 1	4		R19 PC 1	R22 PD 1	N22 PO 1	M10 TE 1	L1 QA 1
Q1	2	2	5		2	2	2	5		2	2	2	2	2
Q2	3	5	5		3	3	3	6		5	5	5	3	5
Q3	4	O23 PB 1	4		4	4	Q23 PB 1	4		6	6	6	4	L2 QA 1
Q4	5	2	5		6	5	2	5		R20 PC 1	R23 PD 1	N23 PD 1	5	2
Q5	6	3	6		6	6	3	6		2	2	2	6	5
Q6	P23 PA 1	O24 PB 1	4		P25 PA 1	P27 PA 1	Q24 PB 1	4		5	5	5	M11 TE 1	L3 QA 1
Q7	2	2	6		2	2	2	5		6	6	6	2	2
Q8	3	3	6		3	3	3	6		R21 PC 1	R24 PD 1	N24 PD 1	3	5
Q9	4	O28 PB 1	4		4	4	Q25 PB 1	4		2	2	2	4	L4 QA 1
Q10	5	2	5		5	5	2	5		5	5	5	5	2
Q11	6	3	6		8	6	3	6		6	6	6	6	5

Q

	III	II	I	IV	II	I	III	II	I	IV	III	II	I	IV
K0	O5 PB 1	4		N7 PA 4	N10 PA 1	P11 PO 1	P8 PA 4	Q8 PB 1	4		R5 PC 8	R12 PD 6	P8 PA 1	N7 PA 1
K1	2	5		5	2	2	5	2	5		R8 PC 1	R13 PD 1	2	2
K2	3	8		6	3	5	6	3	6		2	2	3	3
K3	O9 PB 1	4		N8 PA 4	4	6	P9 PA 4	Q9 PB 1	4		5	5	P9 PA 1	N8 PA 1
K4	2	5		5	5	P12 PD 1	5	2	5		6	6	2	2
K5	5	5		6	6	2	6	3	6		R7 PC 1	R14 PD 1	3	3
K6	O10 PB 1	4		N9 PA 4	N11 PA 1	5	P10 PA 4	Q10 PB 1	4		2	2	P10 PA 1	N9 PA 1
K7	2	5		5	2	6	5	2	5		5	5	2	2
K8	3	6		5	3	P13 PO 6	6	3	6		6	6	3	3

K

CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE

PERIPHERAL AND CONTROL PROCESSOR BARREL MAP

PRODUCT 6601

SIZE C DRAWING NO. 60119300 REV C

SHEET 10 13

STORAGE SEQUENCE CONTROL

Timing for memory references is controlled by the Storage Sequence Control, which is a timing chain of FFs gated by clock pulses. As a "1" passes down the chain, each FF is set for one minor cycle during which it issues commands to the storage logic. This chain reinitiates itself after each cycle and runs continuously. One memory reference is initiated each minor cycle. The Storage Sequence Control overlaps the references as shown in the typical stage "a".

The stages of storage sequence control are numbered according to the processor for which they initiate a memory reference. The commands issued by the first half of a typical stage are:

G → S, Storage a
Clear Z, Storage a + 1
Set Z, Storage a + 5
Enable Sense, Storage a + 7

The second half of state "a" issues the commands:

Read, a
Write, a + 5
Stop Read, a + 6
Stop Write, a + 1

These commands and other signals from storage sequence control define and separate the peripheral and control processors.

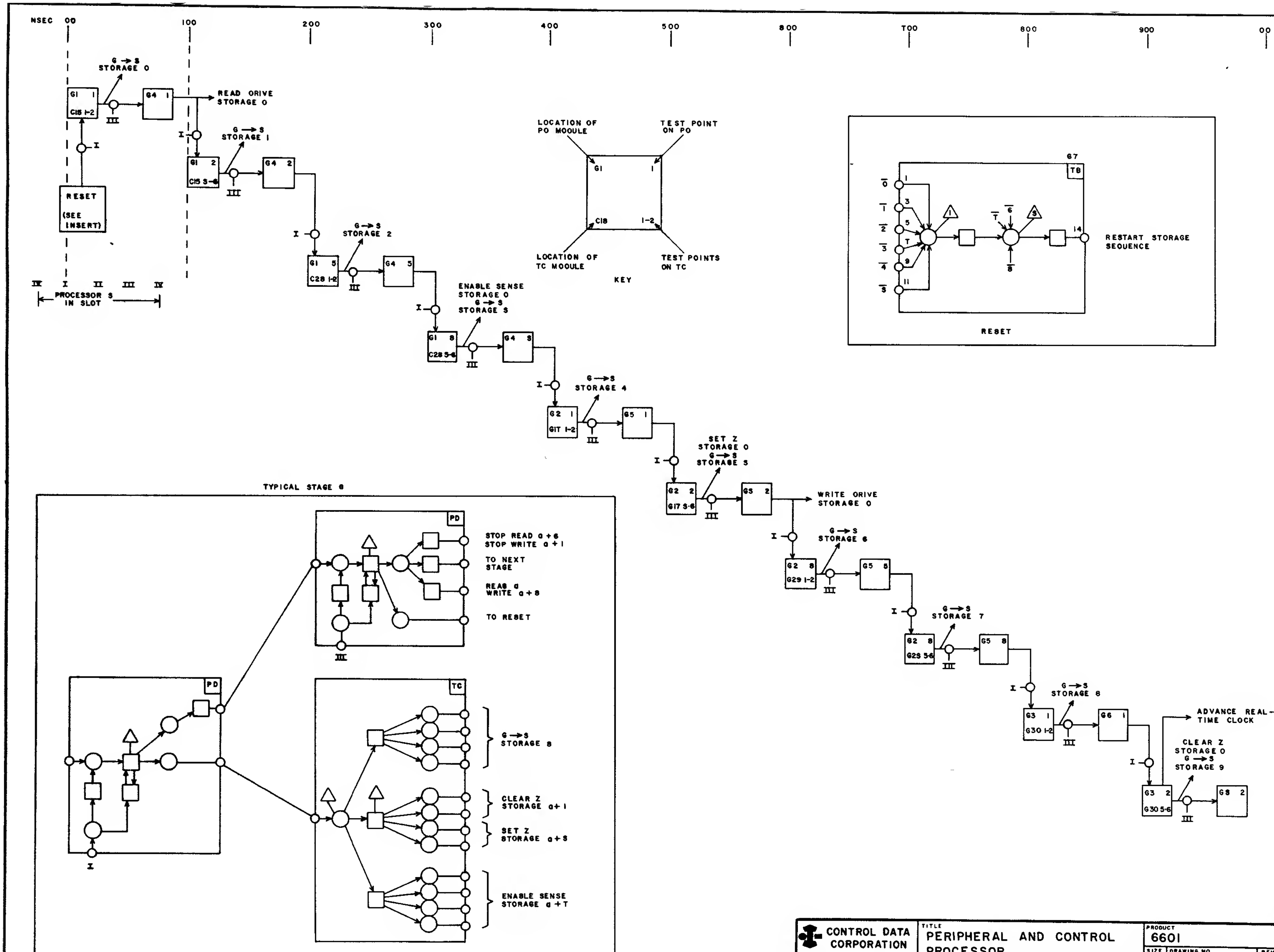
The reset circuit which reinitiates storage sequence control senses whether stages 0-8 are set; if not, stage 0 is reinitiated just after stage 9 has issued its commands.

A memory reference is initiated from stage 6 in the barrel, so that information from memory is available at slot time. Thus, a memory reference for processor 0 (storage 0) is initiated while processor 5 is in the slot.

MEMORY

Each of the ten peripheral and control processors has its own independent core-storage unit with a capacity of 4096 12-bit words. Each has its own address register (S), sense amplifiers, and restoration register (Z). However, the ten storage units share a common memory cycle path and common paths to and from the barrel.

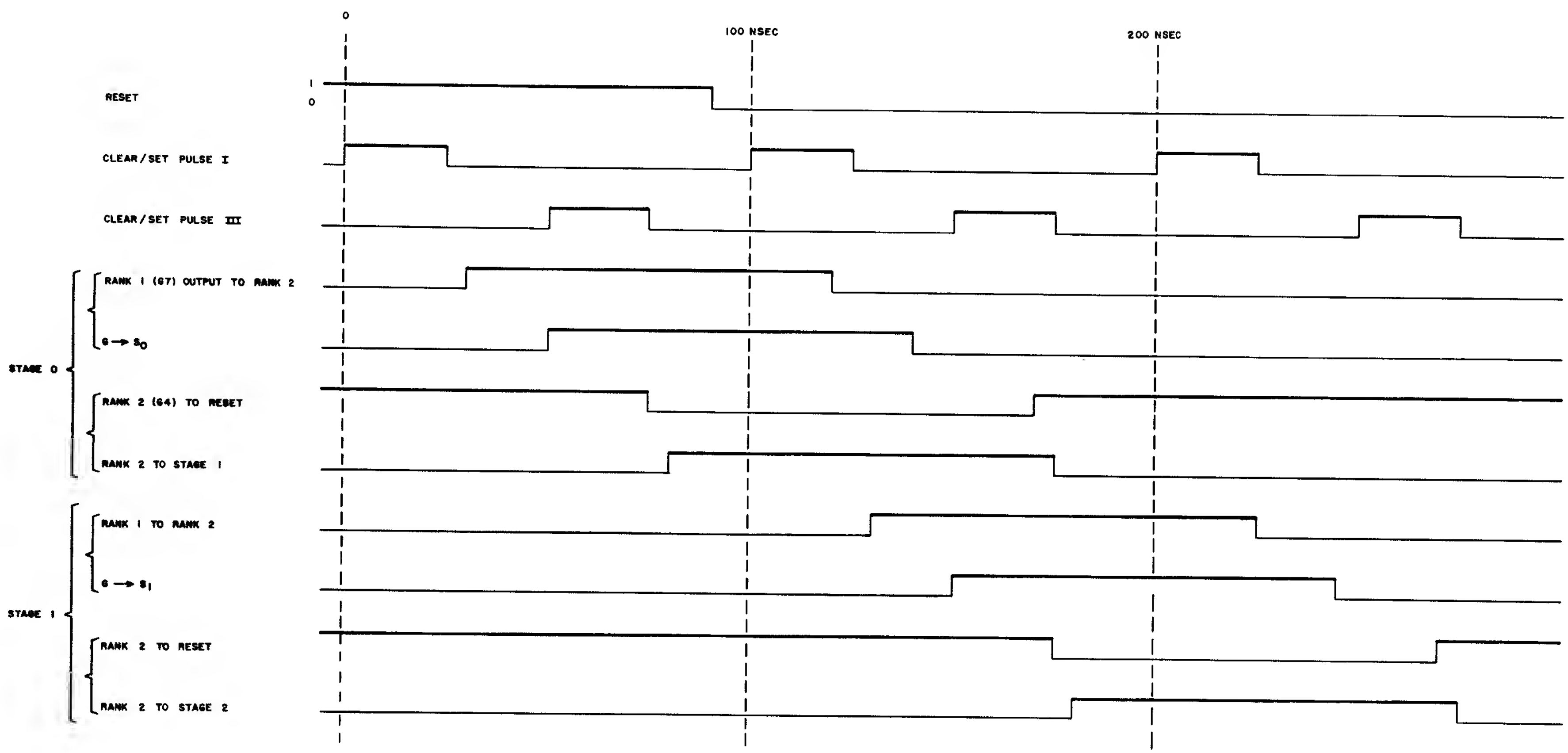
Each peripheral and control processor makes one memory reference each major cycle. When no memory reference is called for by the current instruction, address 0000 is read and restored.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR STORAGE SEQUENCE CONTROL

PRODUCT	SIZE	DRAWING NO.	REV	SHEET	
6601	C	60119300	HD	11	15



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR STORAGE SEQUENCE CONTROL TIMING

PRODUCT: 6601

SIZE: C | DRAWING NO.: 60119300 | REV: C

SHEET: 12 | 17

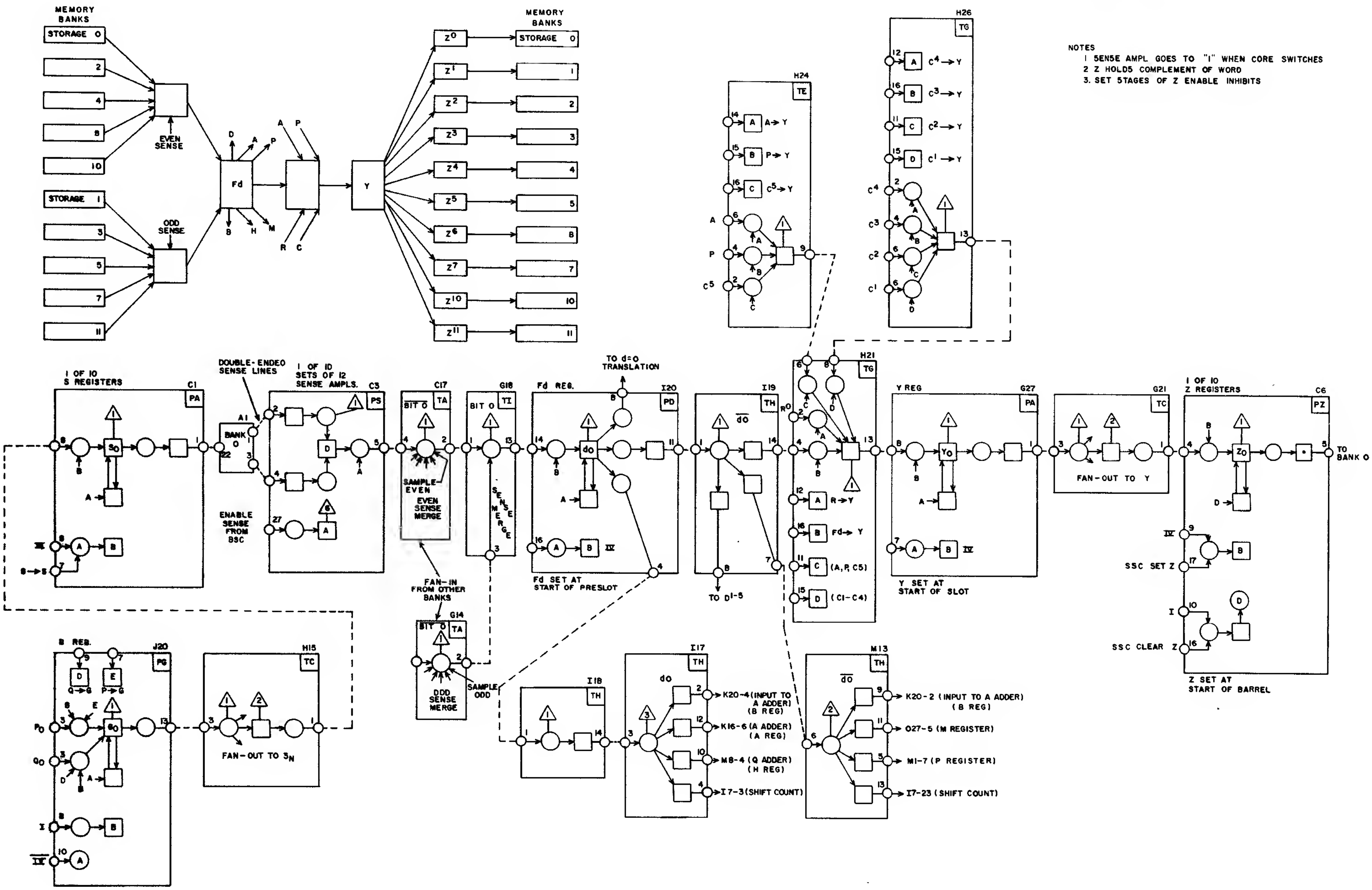
MEMORY CYCLE PATH

The common memory cycle path used by all processors receives data from the memories via the sense merge. Inputs to the sense merge from the sense amplifiers are a logical "1" (0.2v) when sense is not enabled. When a processor's sense amplifiers are enabled, the outputs of the PS modules are allowed to go to +1.2v for a sensed "0". If the core switches, the sense amplifier output goes to +0.2v "1". The AND combination of logical "1's" from unselected processors, even or odd sense enable, and "1" bits from the selected processor's sense amplifiers sets the word from memory into the Fd register in the memory cycle path.

The memory cycle path sends information to the barrel, I/O channels, translators and central write pyramid and receives information from the barrel, central read pyramid, and I/O channels. Outputs from Fd in the memory cycle path are translated and used to form commands when K = 00X (read next instruction trip).

Information in the memory-cycle path (either the read word or a new word) is fanned out from the Y register to the ten Z registers. The set Z signal from storage sequence control gates the complement of the word to be stored into the proper Z register.

NOTES
1 SENSE AMPL GOES TO "1" WHEN CORE SWITCHES
2 Z HOLDS COMPLEMENT OF WORD
3. SET STAGES OF Z ENABLE INHIBITS



CONTROL DATA CORPORATION

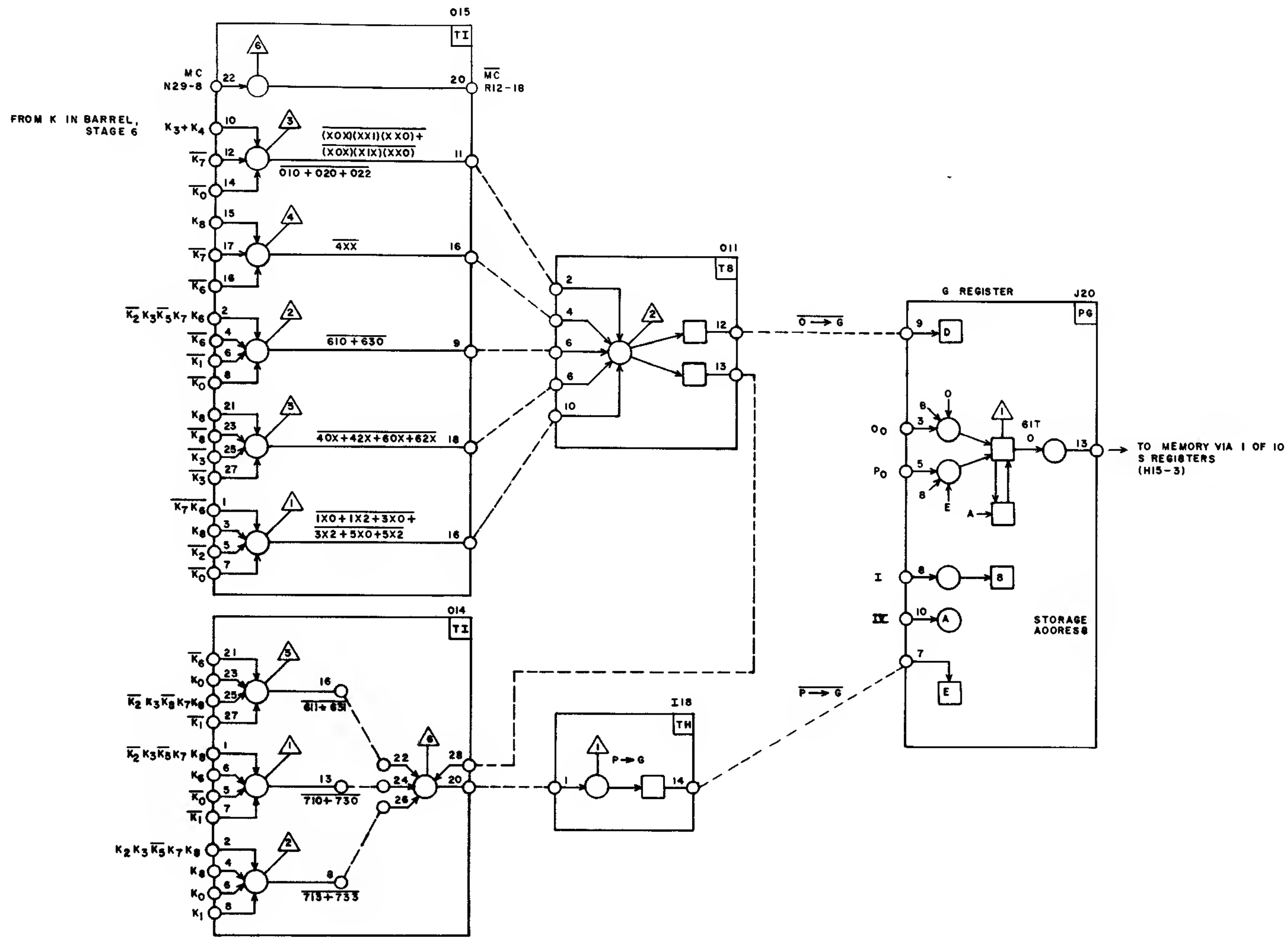
COMPUTER DIVISION

TITLE
PERIPHERAL AND CONTROL PROCESSOR
TYPICAL MEMORY CYCLE PATH

PRODUCT 6601/04

SIZE C | DRAWING NO. 60119300 | REV

SHEET 13 | 19



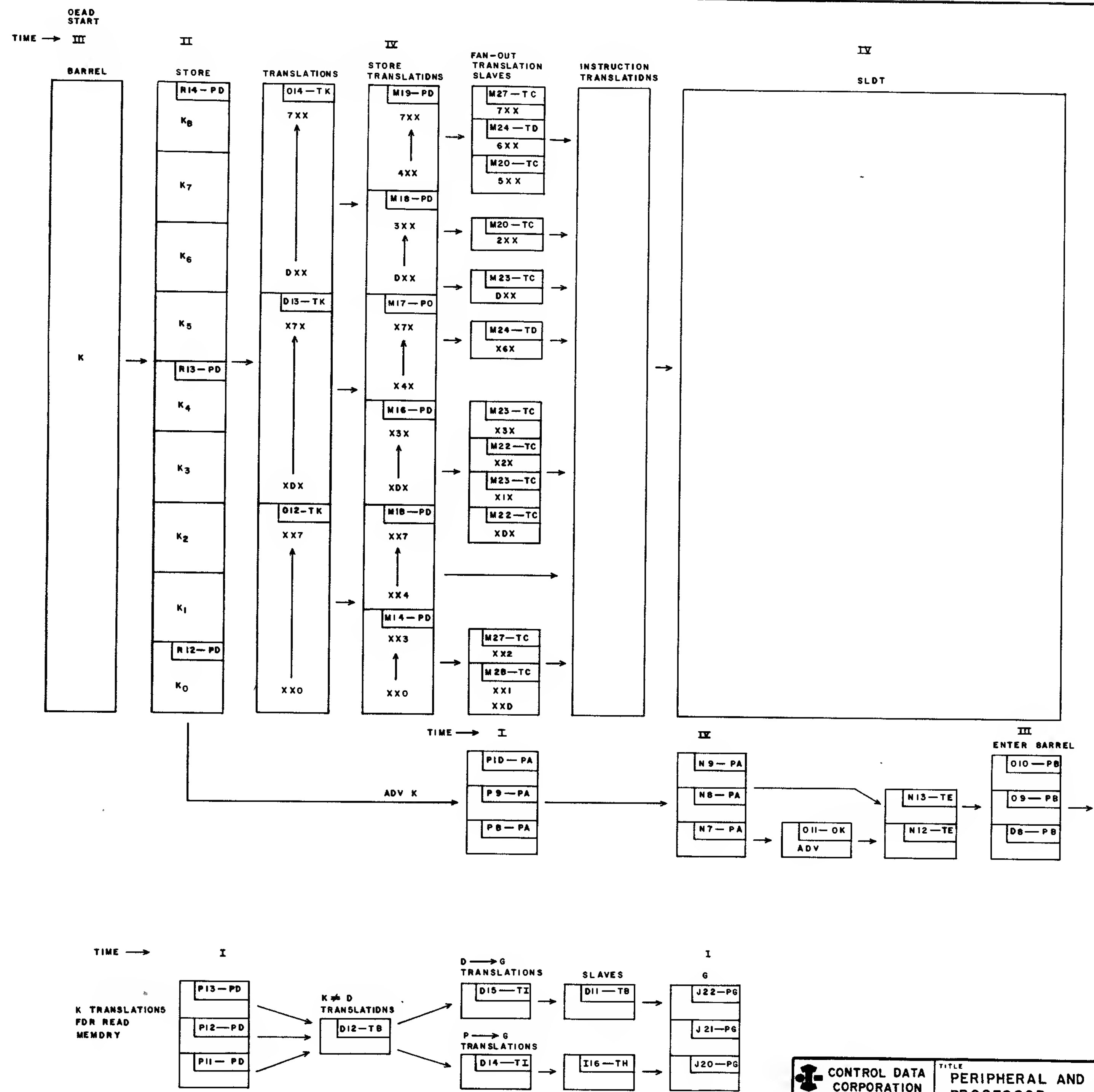
CONTROL DATA CORPORATION	TITLE PERIPHERAL AND CONTROL PROCESSOR	PRODUCT 6601/04
COMPUTER DIVISION	P → G, Q → G	SIZE C DRAWING NO. 60119300 REV BT SHEET 14 21

K REGISTER

K in the slot consists of a 3-bit trip counter for the lower three bits and a fan-in for the upper six bits. The advance K signal to the trip counter is enabled by instruction translations. For some instructions, the advance K signal is controlled by signals which indicate status, i.e., the 5X0 trip is skipped by all 5X instructions if d = 0, and when K = 732, K is advanced only if the I/O channel is empty and active and A = 1.

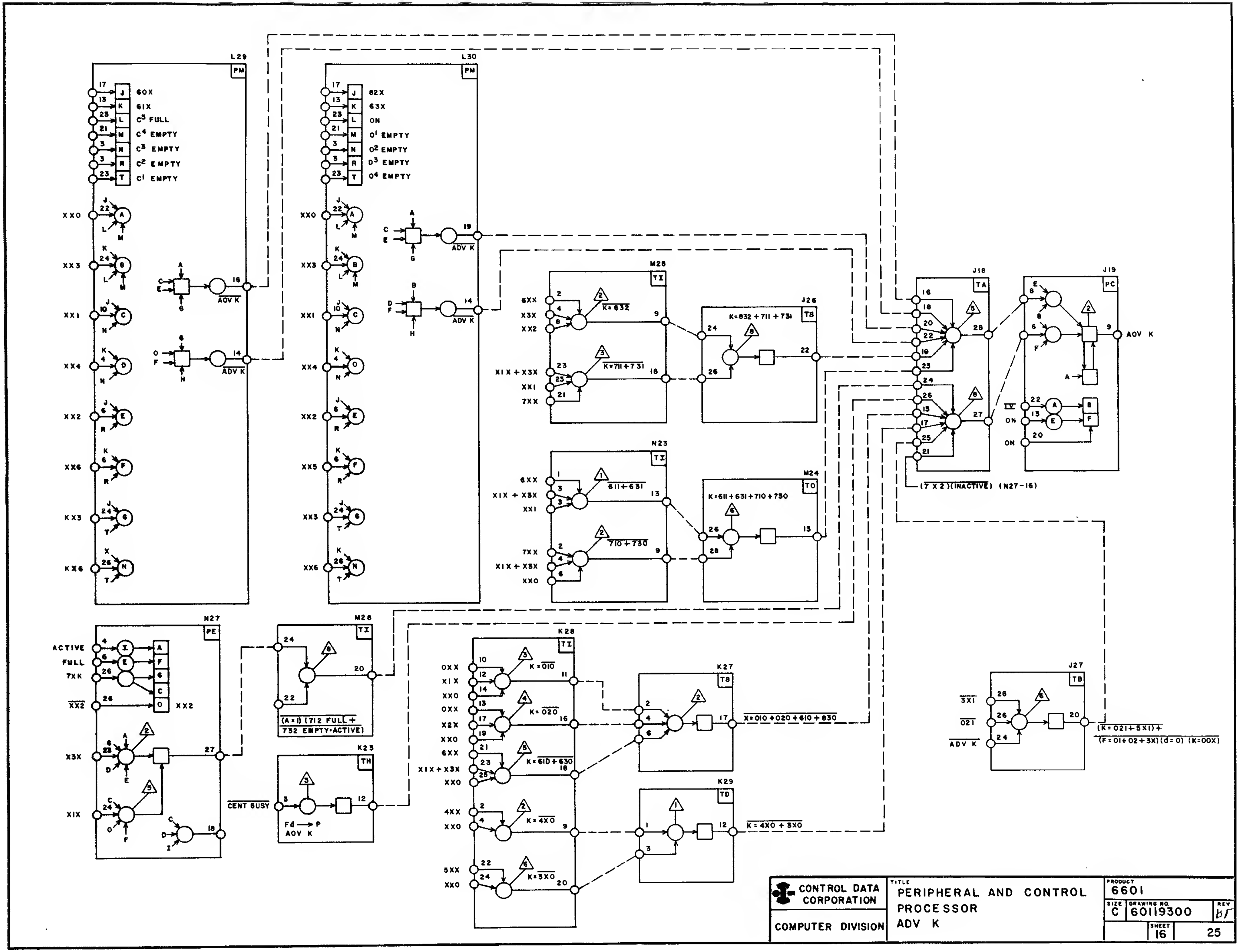
The three-bit trip count controls the sequence of operations for each instruction and is sometimes changed by gates other than the trip counter. For instance, for a central write instruction (63), K is changed from 637 to 633 to repeat the sequence of commands and send another word. When a 63 instruction is completed, K is changed from 637 to 733 to finalize the instruction and obtain the next instruction from storage.

The fan-in to the upper six bits of K allows the instruction code F to be entered into K from storage. The K → K path allows another trip around the barrel for the present instruction. The path K = 340 is used by replace instructions which automatically use the store instruction 34 to accomplish the store portion of the replace instructions.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE	PRODUCT		
PERIPHERAL AND CONTROL PROCESSOR K TRANSLATIONS, GENERAL	6601		
SIZE: C	DRAWING NO: 60119300	REV: BD	
	SHEET 15	23	



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR ADV K

PRODUCT: 6601

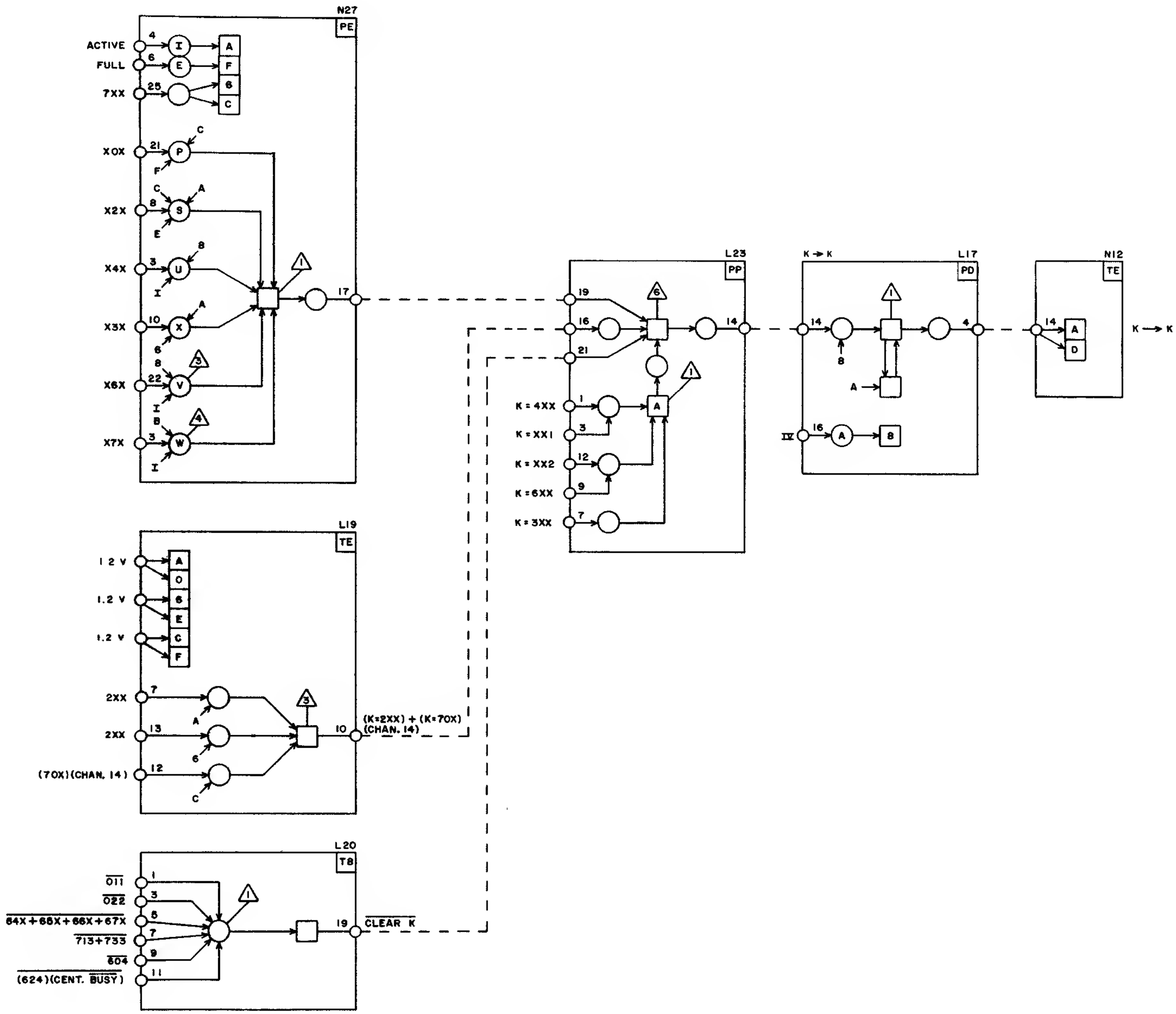
SIZE: C

DRAWING NO: 60119300

REV: b7

SHEET: 16

25



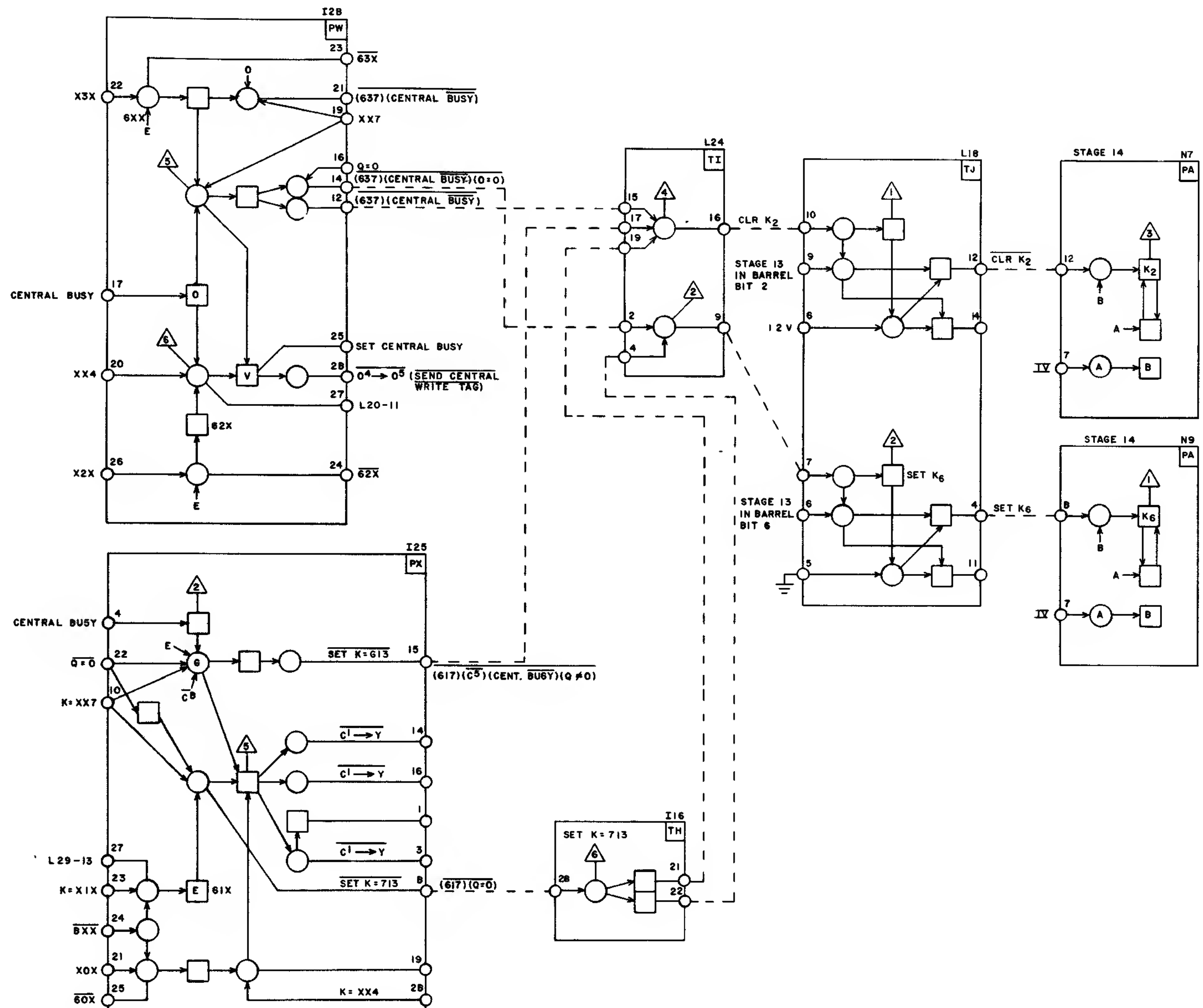
CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE

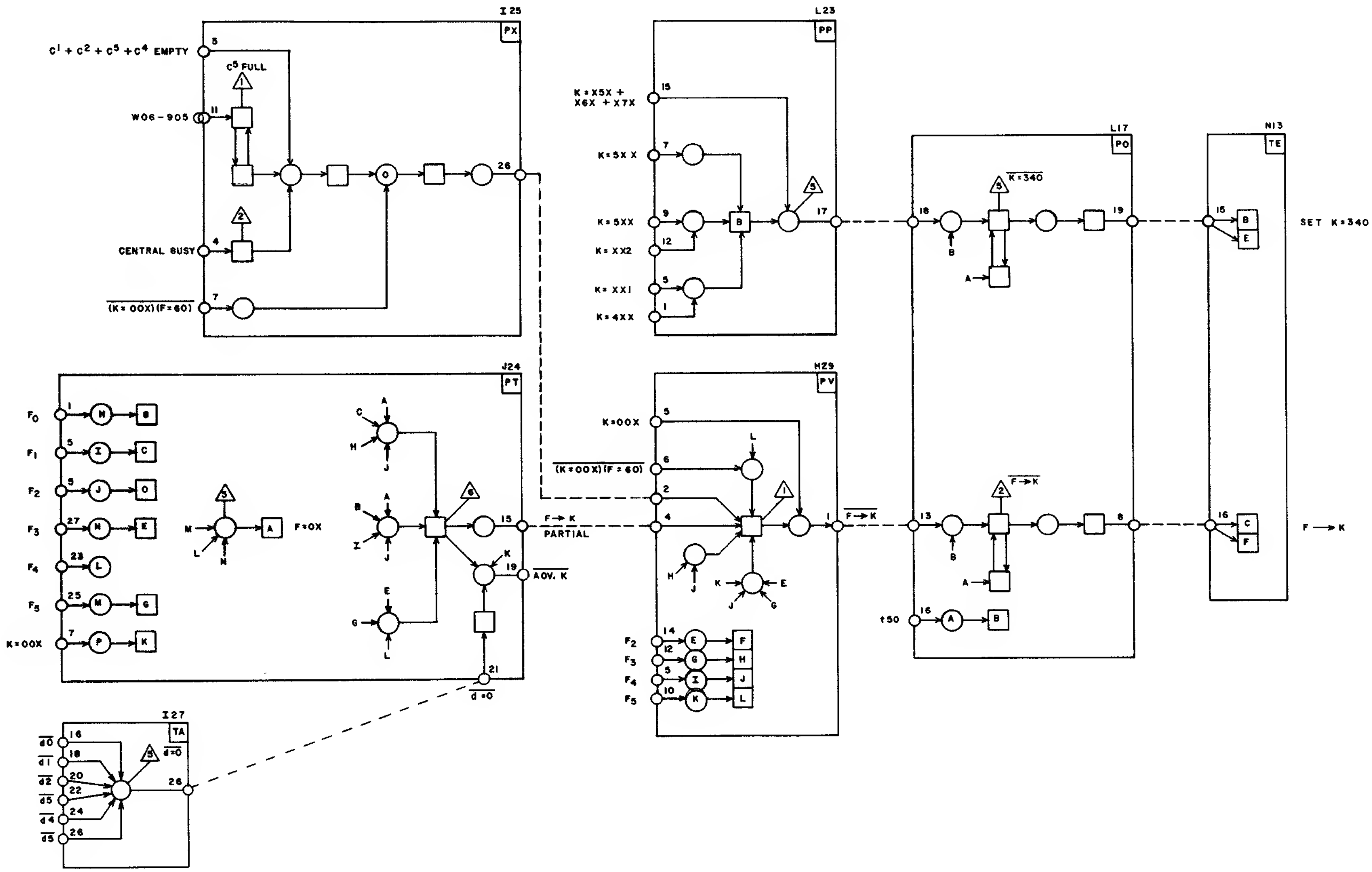
PERIPHERAL AND CONTROL PROCESSOR
K → K GATE

PRODUCT 6601		
SIZE C	DRAWING NO. 60119300	REV D
	SHEET 17	27



NOTE
1 I16 TP 5 CKT USED ON SERIALS 1-7

CONTROL DATA CORPORATION	TITLE PERIPHERAL AND CONTROL PROCESSOR CLR K_2, SET K_6	PRODUCT 6601
COMPUTER DIVISION		SIZE C DRAWING NO. 60119300 REV 6F SHEET 18 29

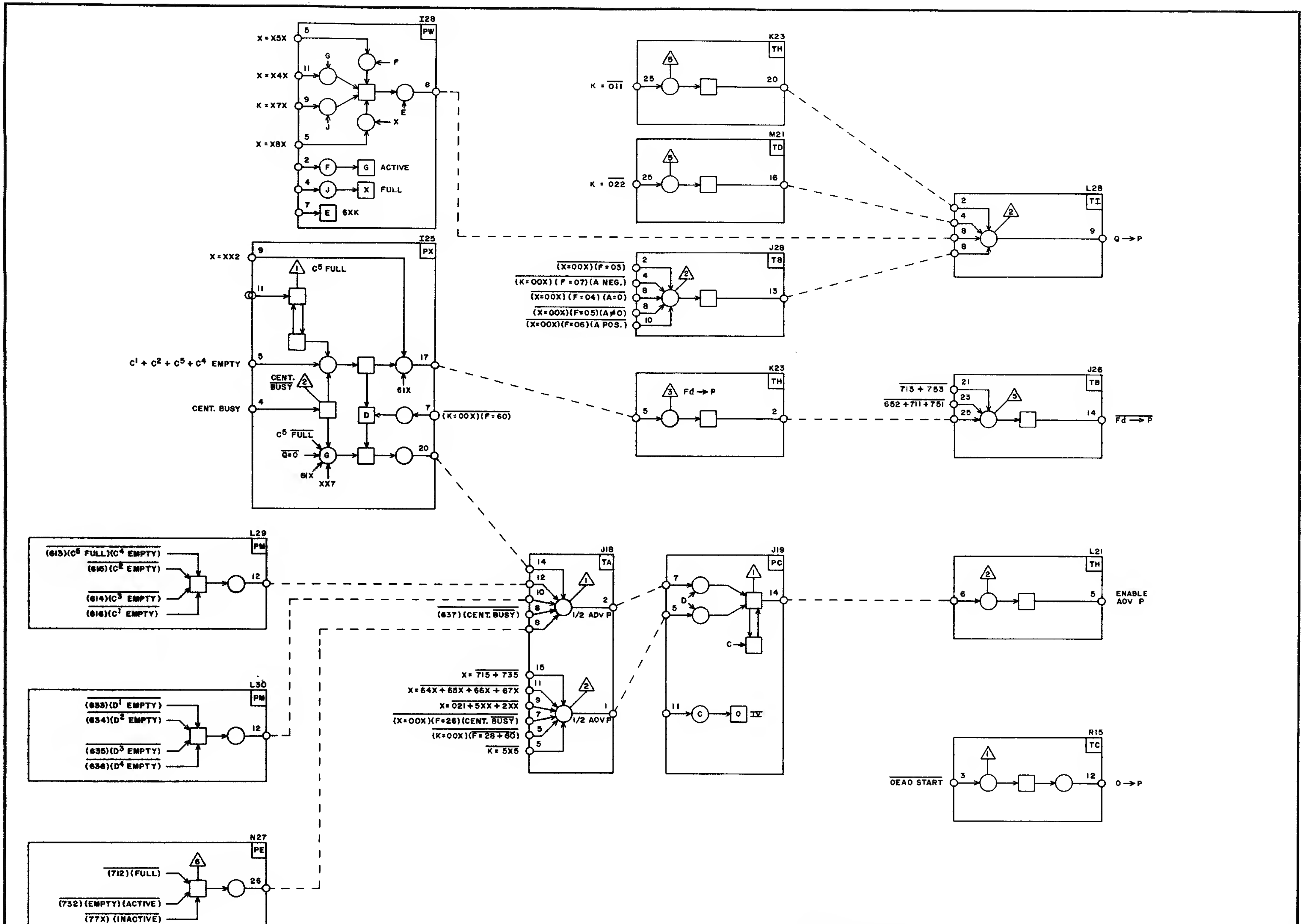


CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE PERIPHERAL AND CONTROL PROCESSOR SET K=340, F → K GATES

PRODUCT		
6601		
SIZE C	DRAWING NO. 60119300	REV BT
	SHEET 19	31



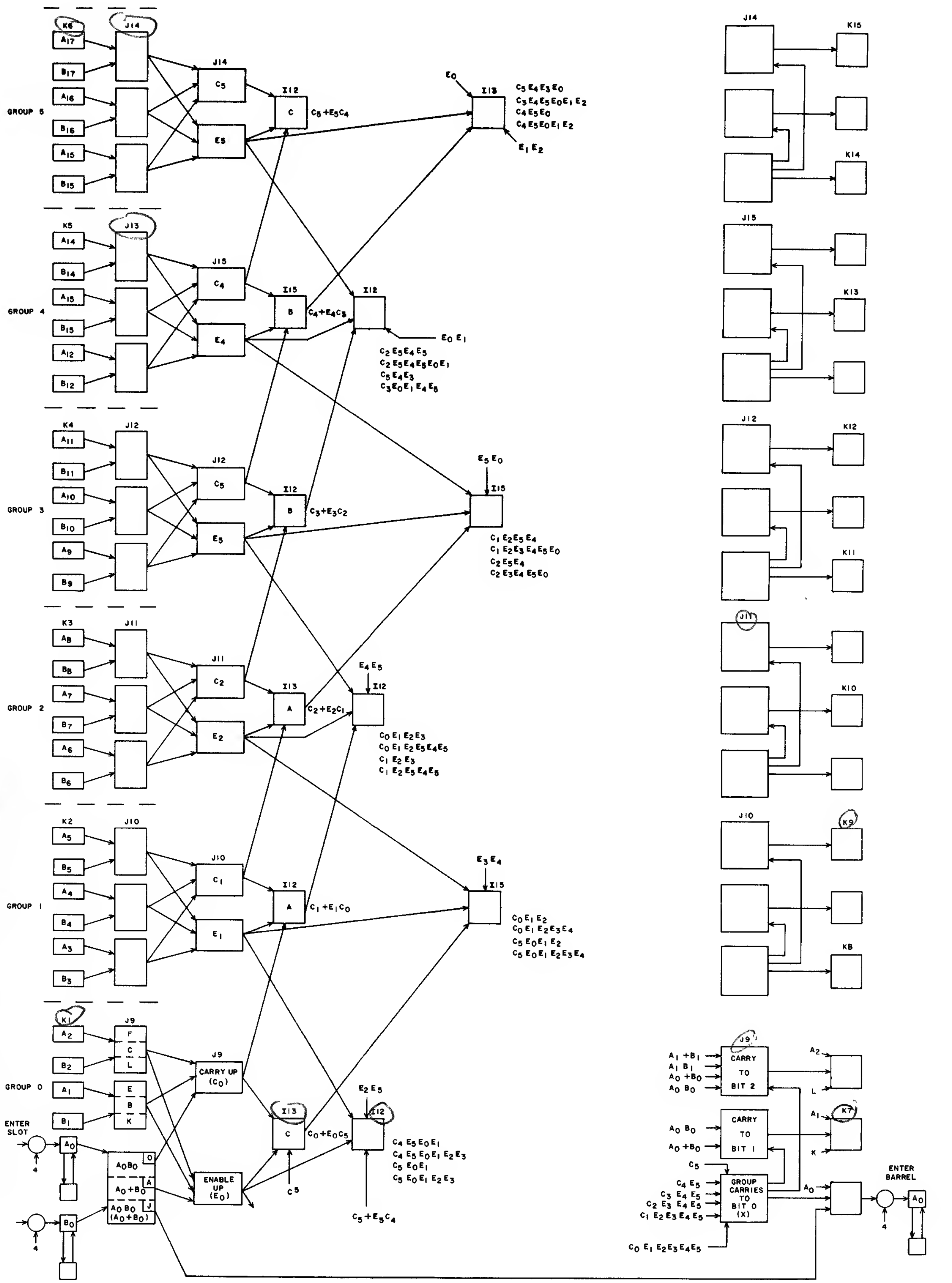
CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE

PERIPHERAL AND CONTROL PROCESSOR
P REGISTER GATES

PRODUCT 6601		
SIZE C	DRAWING NO. 60119300	REV D
	SHEET 20	33



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE PERIPHERAL AND CONTROL PROCESSOR A ADDER, OVER-ALL BLOCK DIAGRAM

PRODUCT	SIZE	DRAWING NO.	REV	SHEET	
6601	C	60119300	C	21	35

A ADDER

The A adder is used to execute add, subtract, selective clear, logical product, and logical difference instructions. Parts of the A adder are also used to enter a word into the shift network and gate the result back to the barrel. The quantity in A in the barrel is always complemented when it enters the slot. When no operation on A is called for, (A) is complemented, enters the A adder, is added to zero, and the result is recomplemented at the output. The Add gate on the QD modules is always enabled except when Selective Clear, Logical Product, or Shift commands are enabled.

Add

For an add instruction (A) is complemented and entered into the A input register. The second operand is also complemented and entered into the B input register. The two quantities in the input registers, taken as positive, are added and the sum is re-complemented as it is gated out of the QD modules to the barrel.

Subtract

For subtract instructions, the minuend, (A) is complemented as it enters the adder. The subtrahend is entered into B without being complemented and the two quantities are added as in an add instruction.

Selective Clear

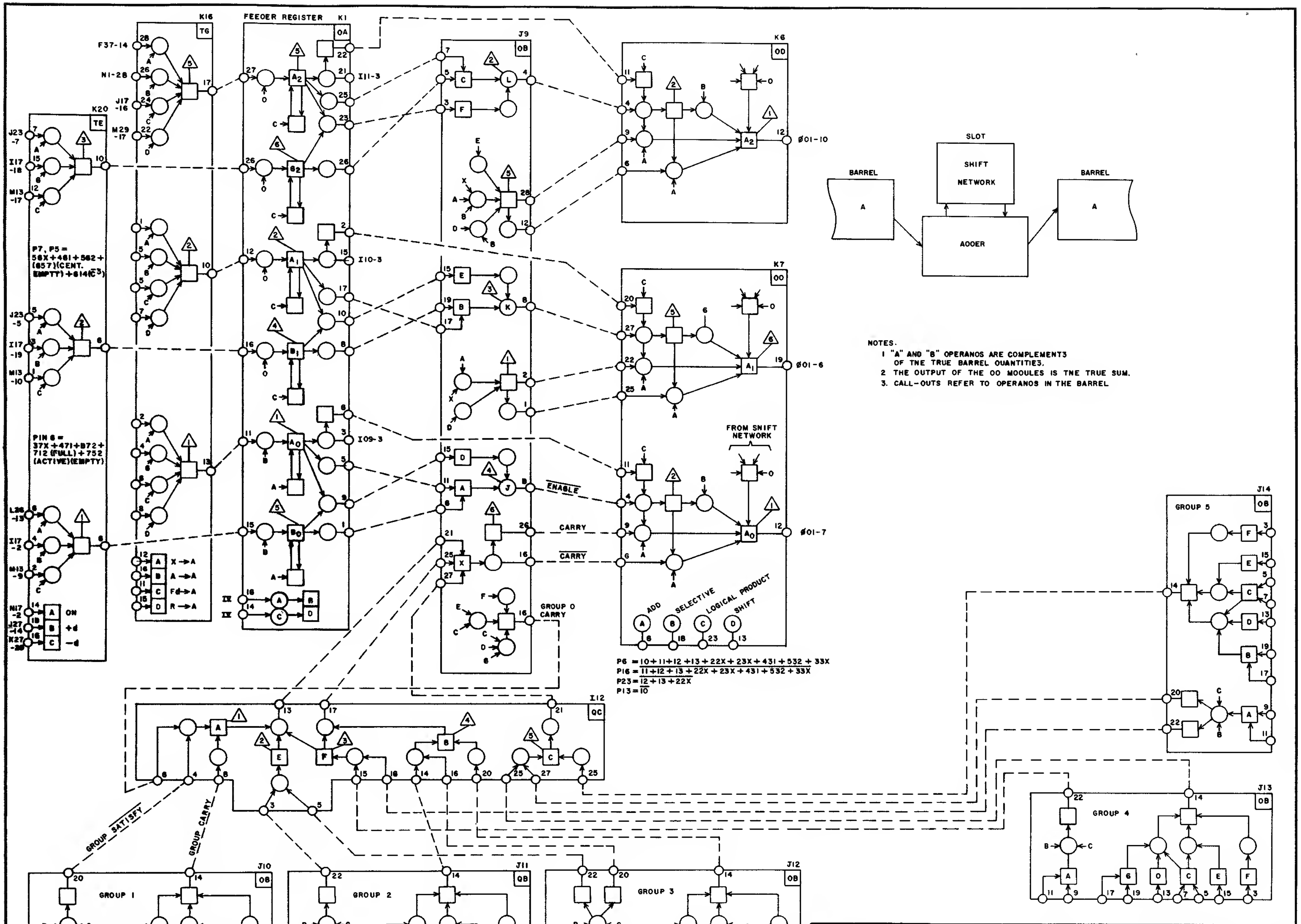
For selective clear, the complement of A and the true value of d are entered into the adder and both the selective and the logical product gates are enabled.

Logical Product

For logical product instructions, both A and d (or dm) are complemented before entering the adder and both the logical product and the selective gates are enabled.

Logical Difference

For logical difference instructions, the complement of A and the true value of the second operand enter the adder and only the selective gate is enabled.



NOTES.
1 "A" AND "B" OPERANDS ARE COMPLEMENTS OF THE TRUE BARREL QUANTITIES.
2 THE OUTPUT OF THE 00 MODULES IS THE TRUE SUM.
3. CALL-OUTS REFER TO OPERANDS IN THE BARREL

$P6 = 10+11+12+13+22X+23X+431+532+33X$

$P16 = \overline{11+12+13+22X+23X+431+532+33X}$

$P23 = \overline{12+13+22X}$

$P13 = \overline{10}$

CONTROL DATA CORPORATION

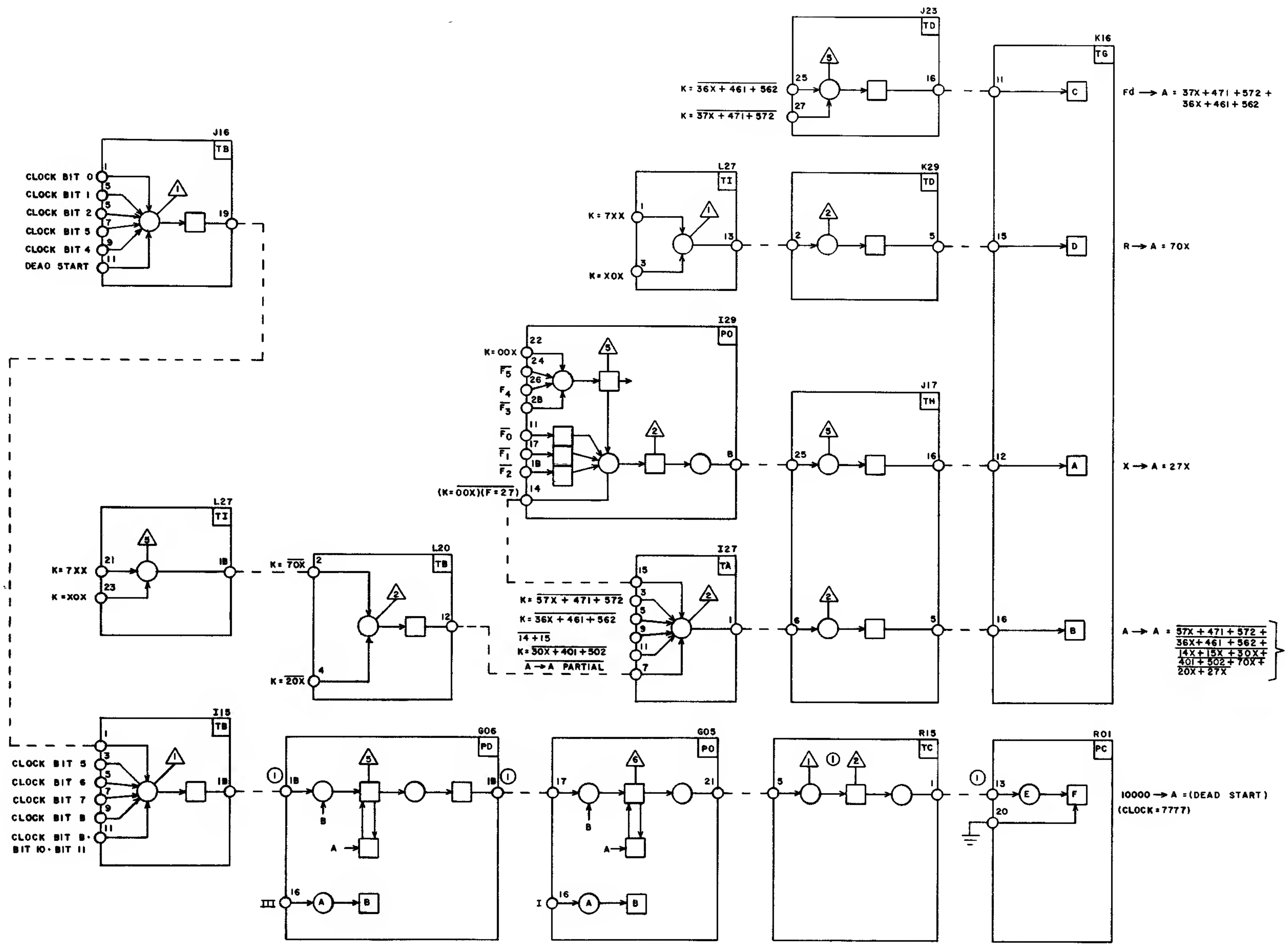
COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR A ADDER

PRODUCT: 6601

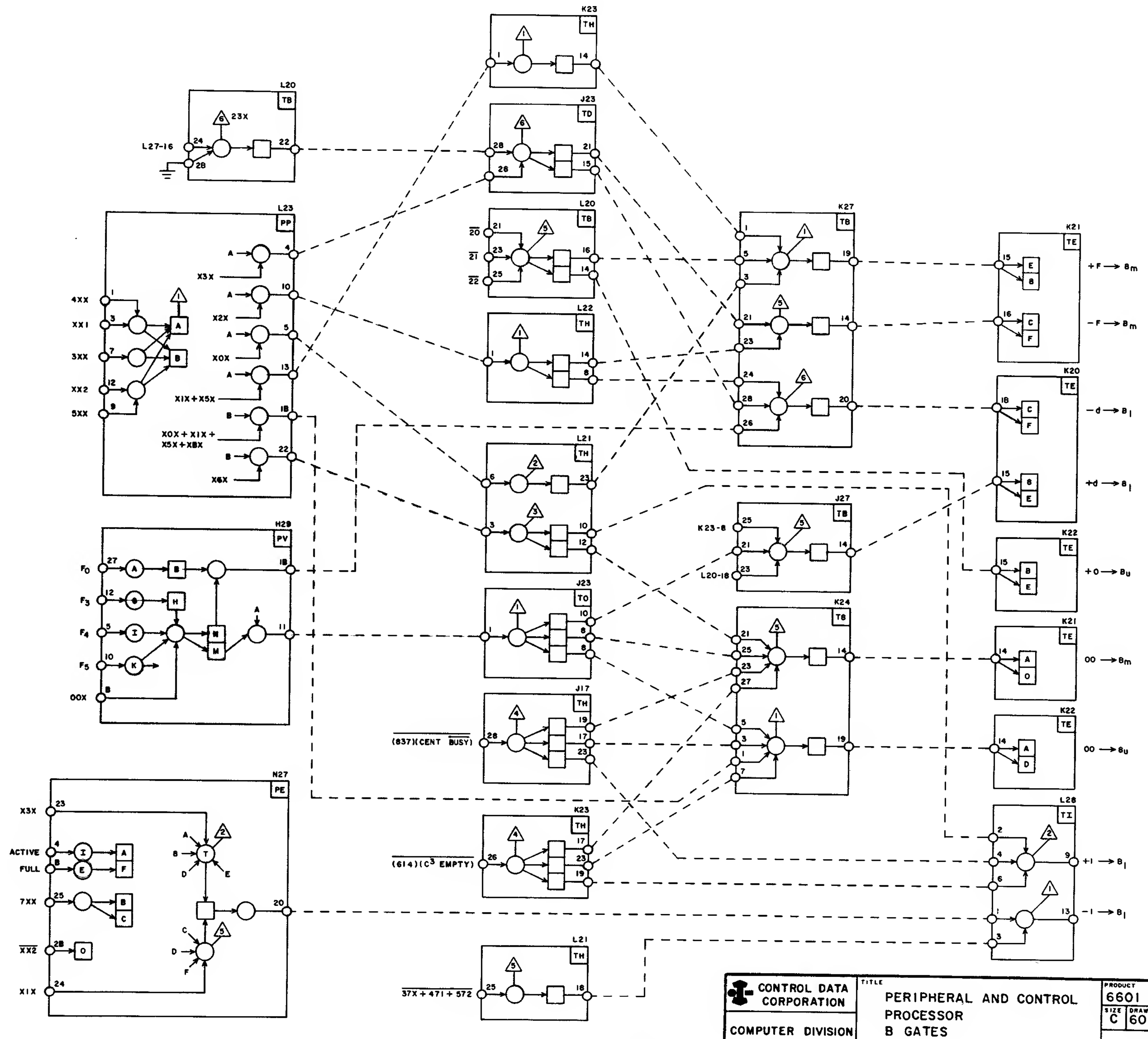
SIZE: C | DRAWING NO. 60119300 | REV: HT

SHEET 22 | 37

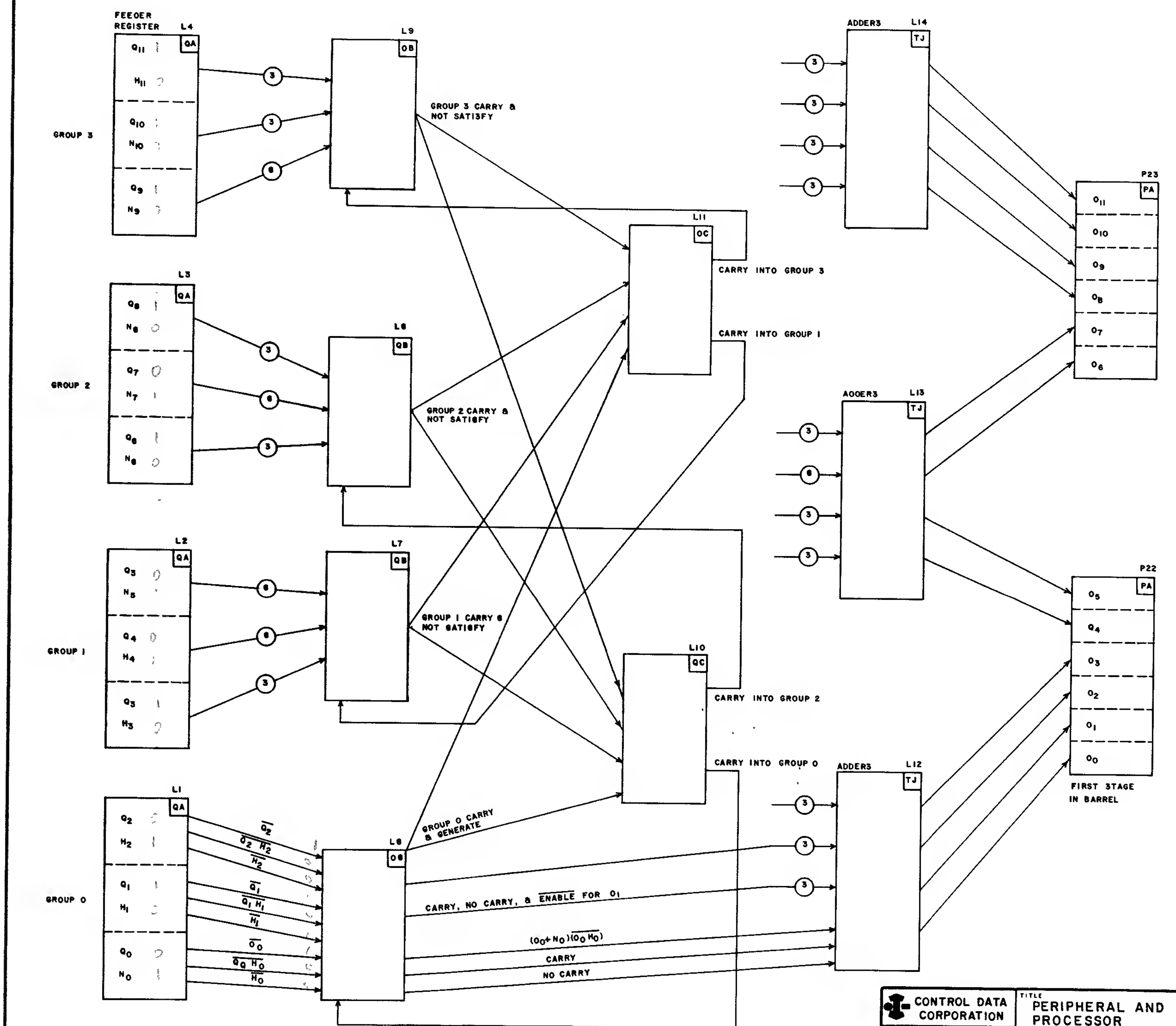


NOTES:
(1) DEAD START.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR A REGISTER GATES	PRODUCT 6601/04 SIZE C · DRAWING NO. 60119300 · REV BT SHEET 23 · 39



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR B GATES	PRODUCT 6601 SIZE C · DRAWING NO. 60119300 · REV BT SHEET 24 · 41

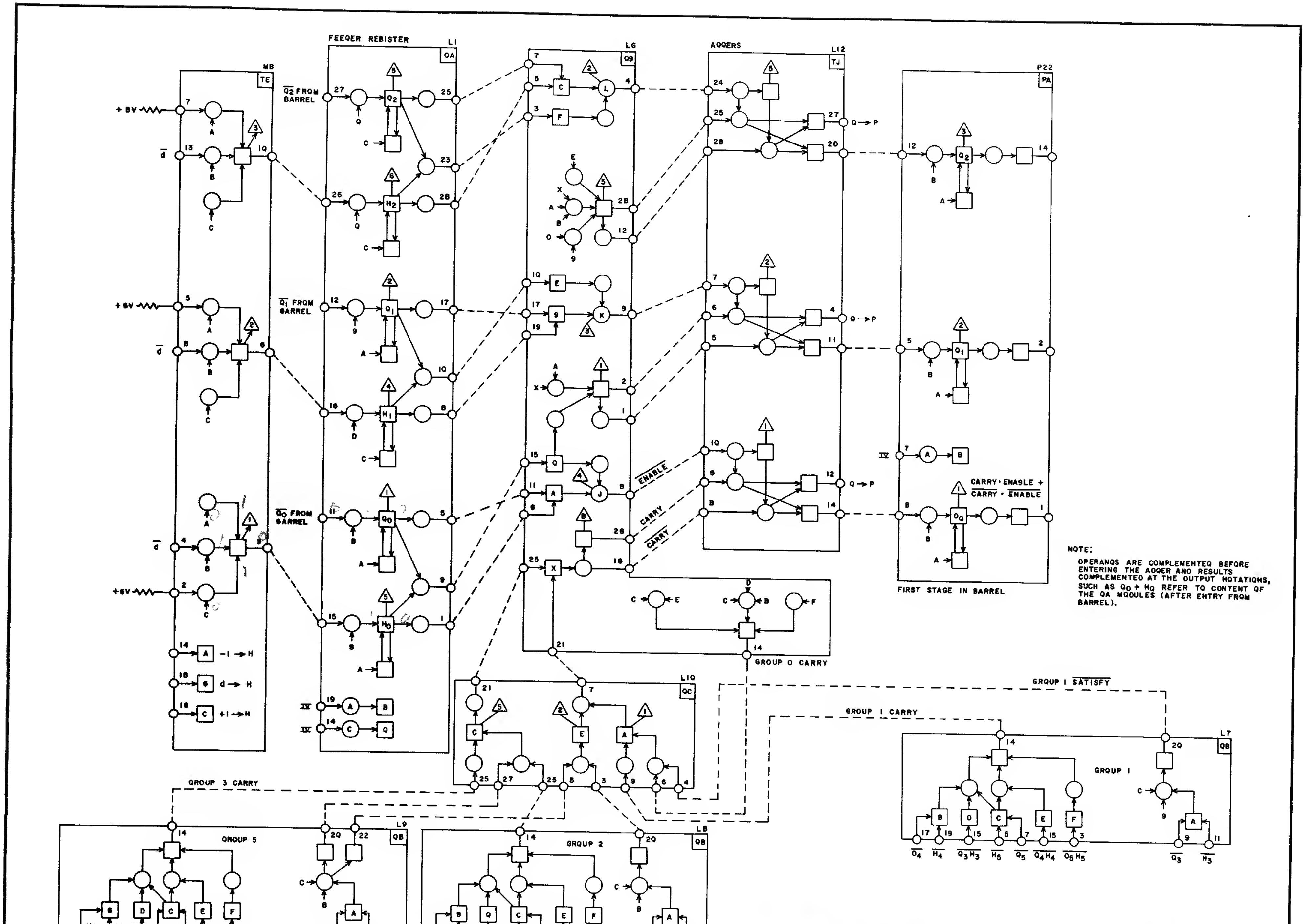


NOTE:
OPERANDS ARE COMPLEMENTED BEFORE ENTERING ADDER AND RESULT IS COMPLEMENTED AT THE OUTPUT. NOTATIONS SUCH AS $O_0 + N_0$ REFER TO CONTENT OF THE QA MODULES (AFTER ENTRY FROM BARREL).

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR Q ADDER BLOCK DIAGRAM

PRODUCT: 6601
SIZE: C
DRAWING NO. 60119300
REV: C
SHEET: 25
43



CONTROL DATA CORPORATION

COMPUTER DIVISION

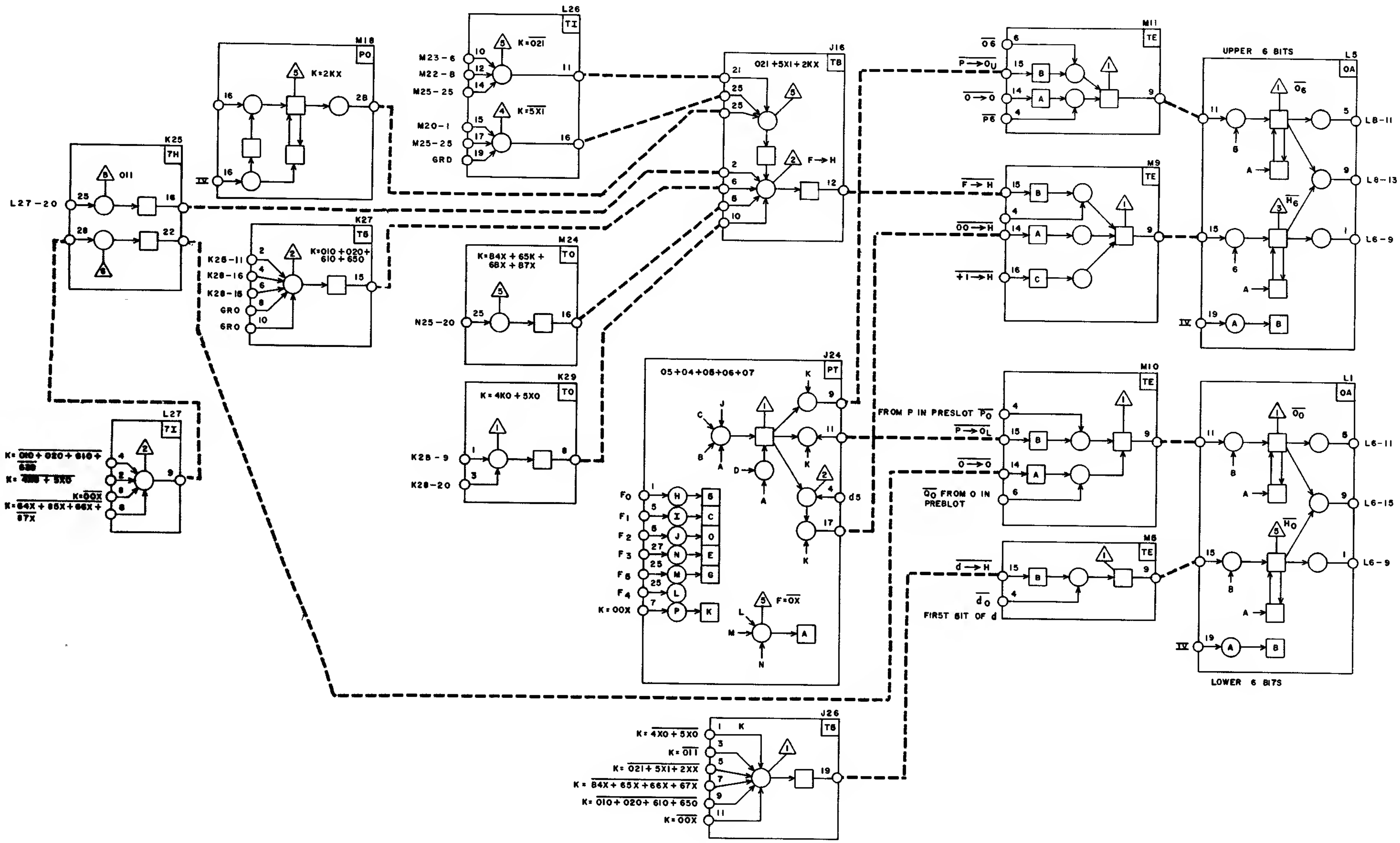
TITLE

PERIPHERAL AND CONTROL PROCESSOR
Q ADDER

PRODUCT 6601

SIZE C | DRAWING NO. 60119300 | REV D

SHEET 26 | 45



CONTROL DATA CORPORATION

COMPUTER DIVISION

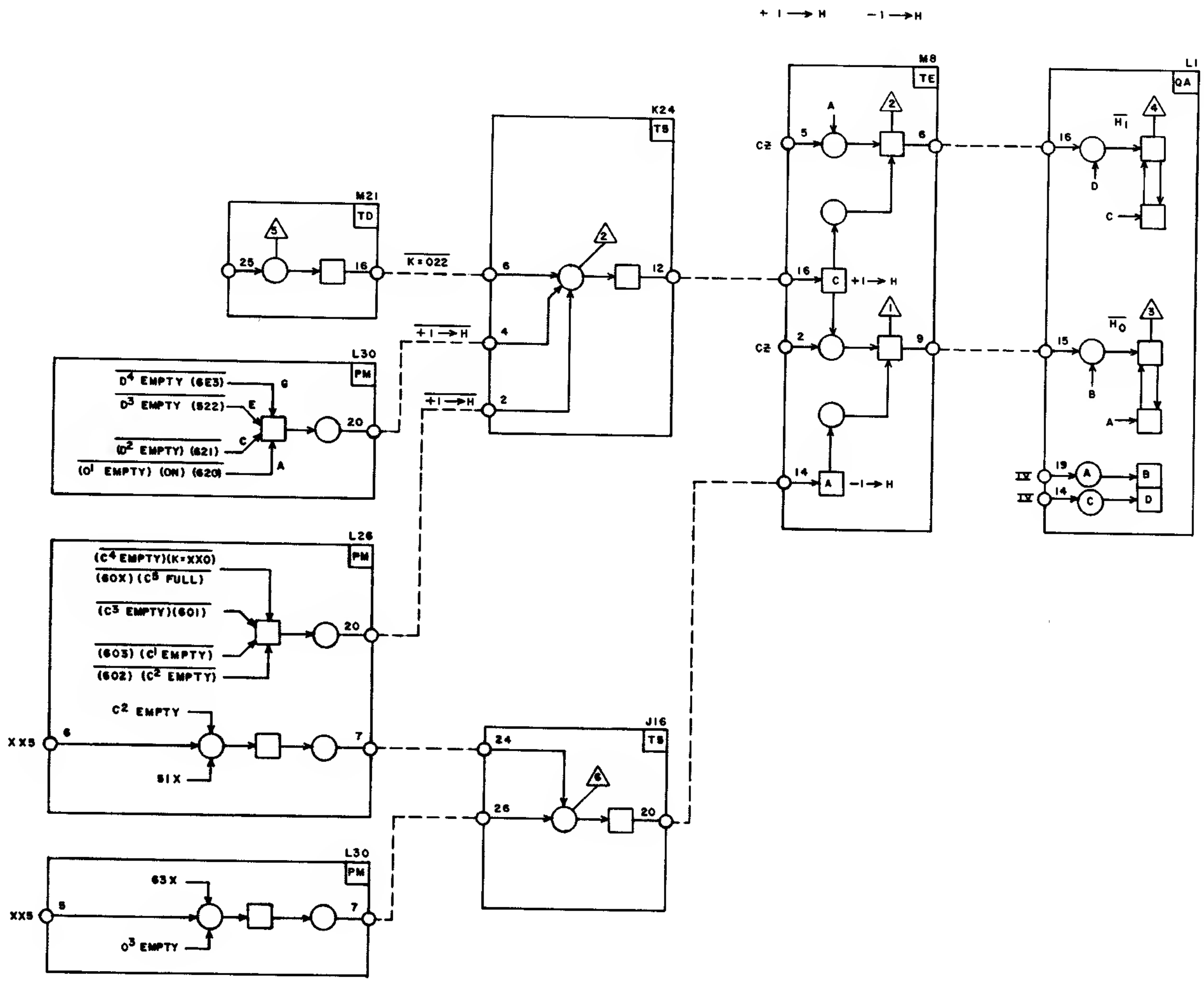
TITLE

PERIPHERAL AND CONTROL PROCESSOR
Q AND H REGISTER GATES

PRODUCT 6601/04

SIZE C | DRAWING NO. 60119300 | REV BT

SHEET 27 | 47



CONTROL DATA CORPORATION	TITLE PERIPHERAL AND CONTROL PROCESSOR H GATES	PRODUCT 6601
COMPUTER DIVISION		SIZE C · DRAWING NO. 60119300 · REV · SHEET 28 · 49

SHIFT NETWORK

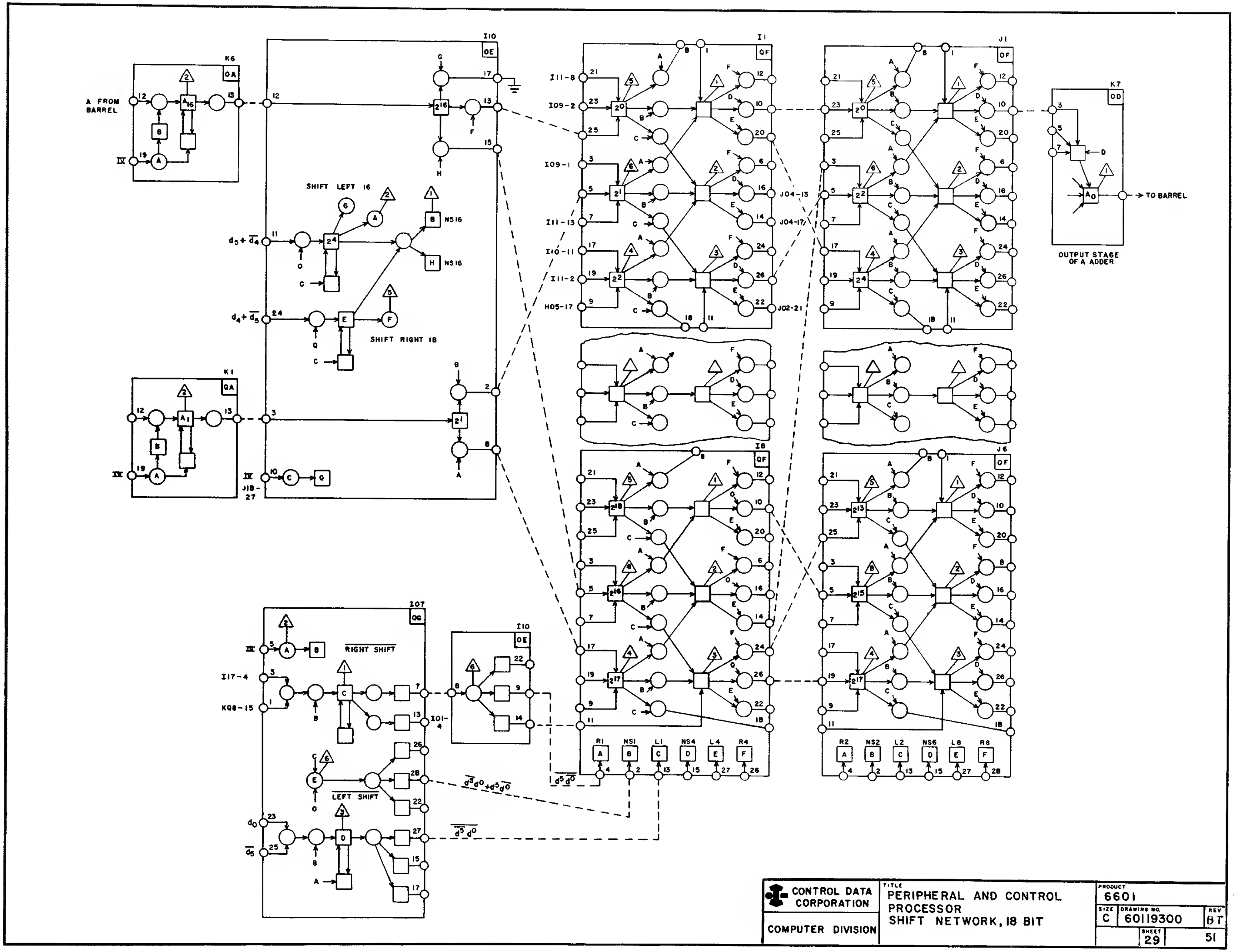
The shift instruction (10) provides for shifting the number in A up to 31 places left or right. Left shift is circular with the high order bits re-entering A at the low-order end. Right shift is end-off with low-order bits discarded as they shift out of the A register and with no sign extention. Thus, a left shift of 18 is equivalent to no shift, and a right shift of 18 clears the A register.

The shift network is a static network. The content of A enters the register at time IV, each bit follows a path established by static translations of the 6-bit shift count in d, and the result re-enters A in the barrel at the next time IV. The input to the shift network comes from the A input register in the A adder (the content of that register, which is the complement of A, is re-complemented before entering the shift register). The output of the shift network is gated back to the barrel by way of the output modules (QD) of the A adder. Note that the quantity in A is always shifted but the result is gated to the barrel only when the current instruction is a shift.

If d is positive ($00-37_8$) the shift is left and the shift count is the content of d. If d is negative ($40-77_8$) the shift is right and the shift count is the complement of the number in d.

At the first stage of the shift network, d_4 and d_5 are tested to determine whether the shift is greater or less than 16 and whether it is right or left. If the shift is 16 or greater, a shift of 16 is made at this point and the result then enters the rest of the shift network.

Bits d_0-d_3 are tested with d_5 to set up paths through the rest of the network.


A FROM BARREL
SHIFT LEFT 16
SHIFT RIGHT 18
RIGHT SHIFT
LEFT SHIFT
OUTPUT STAGE OF A ADDER
TO BARREL
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
PERIPHERAL AND CONTROL PROCESSOR
SHIFT NETWORK, 18 BIT
PRODUCT 6601
SIZE C
DRAWING NO. 60119300
REV BT
SHEET 29
51

COMMUNICATION WITH CENTRAL MEMORY AND CENTRAL PROCESSOR

The peripheral and control processors may communicate with the central processor and central memory in several ways. They may read the central processor's program address, tell the central processor to jump to given central memory address for its next instruction, or read from or write into central memory.

CENTRAL PROGRAM MONITOR

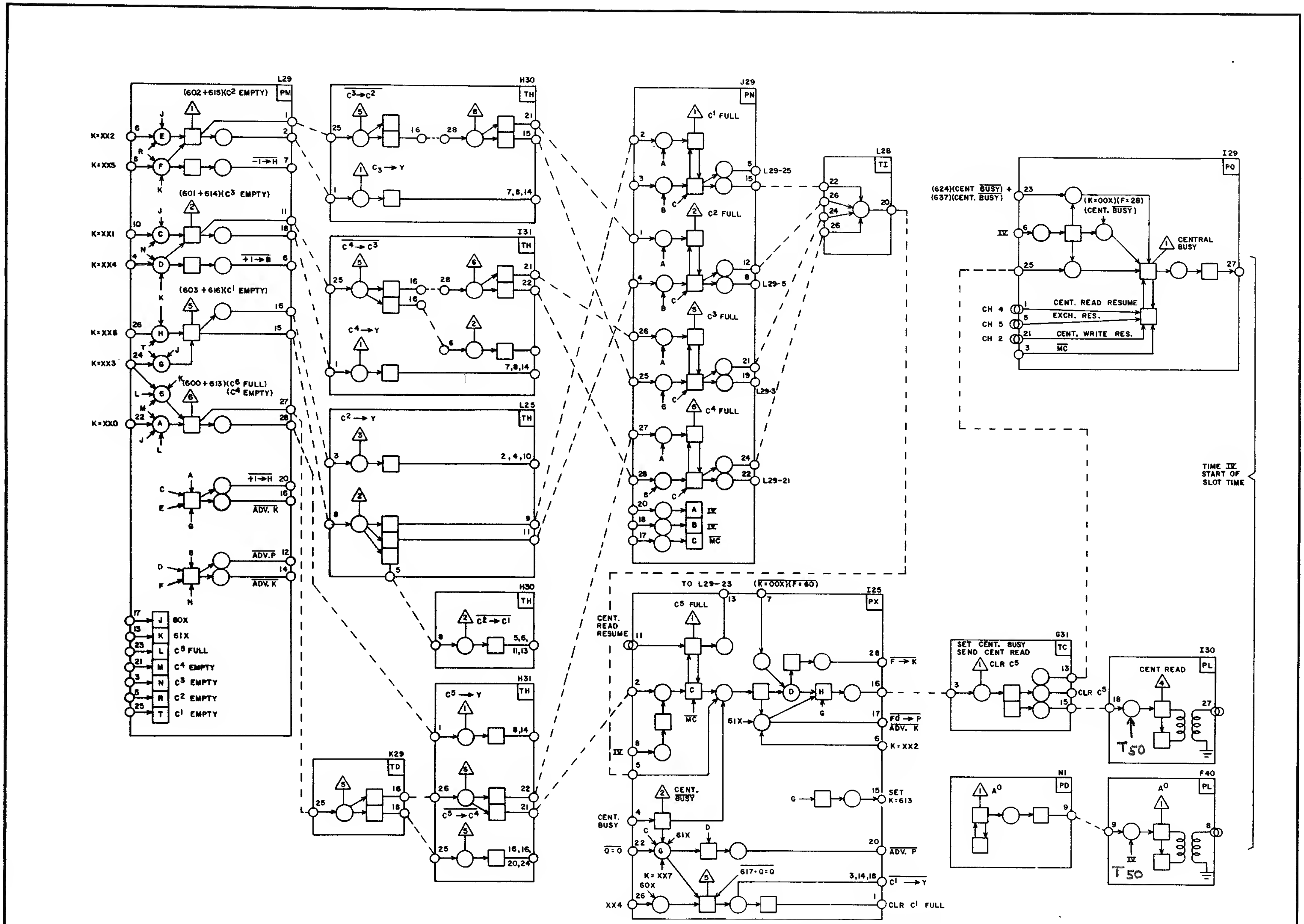
The 18-bit central processor program address is sent to the central program monitor register on chassis 1 every minor cycle. A Read Program Address instruction (27) sends the central address to the A register. Thus the progress of a central program may be monitored by any peripheral and control processor.

Exchange Jump, Central Read, and Central Write instructions all use the content of A as a central memory address. (A) is unconditionally sent to address control in the central processor every minor cycle. This quantity is recognized and used as a central memory address only if accompanied by a Central Read, Central Write, or Exchange Jump signal.

The Central Busy FF indicates when a reference to central is in progress. A central Busy condition prevents initiating a central reference until one in progress is completed.

EXCHANGE JUMP

An exchange jump instruction is used to command the central processor to stop the program it is executing and go to a central memory location specified by the instruction. An exchange jump may be issued by any peripheral and control processor so long as the Central Busy FF is clear. The instruction sends an Exchange Jump signal to the central processor and sets the Central Busy FF. The Exchange Jump signal tells the central processor to recognize the 18-bit address sent from the peripheral processor and to perform an exchange jump. After the central processor has performed the exchange jump and started a new program it sends a Resume signal which clears the Central Busy FF to allow another central reference. If a peripheral and control processor tries to issue an Exchange Jump instruction while the Central Busy FF is set, the processor must wait until the previous central reference is completed and the Central Busy FF is cleared.

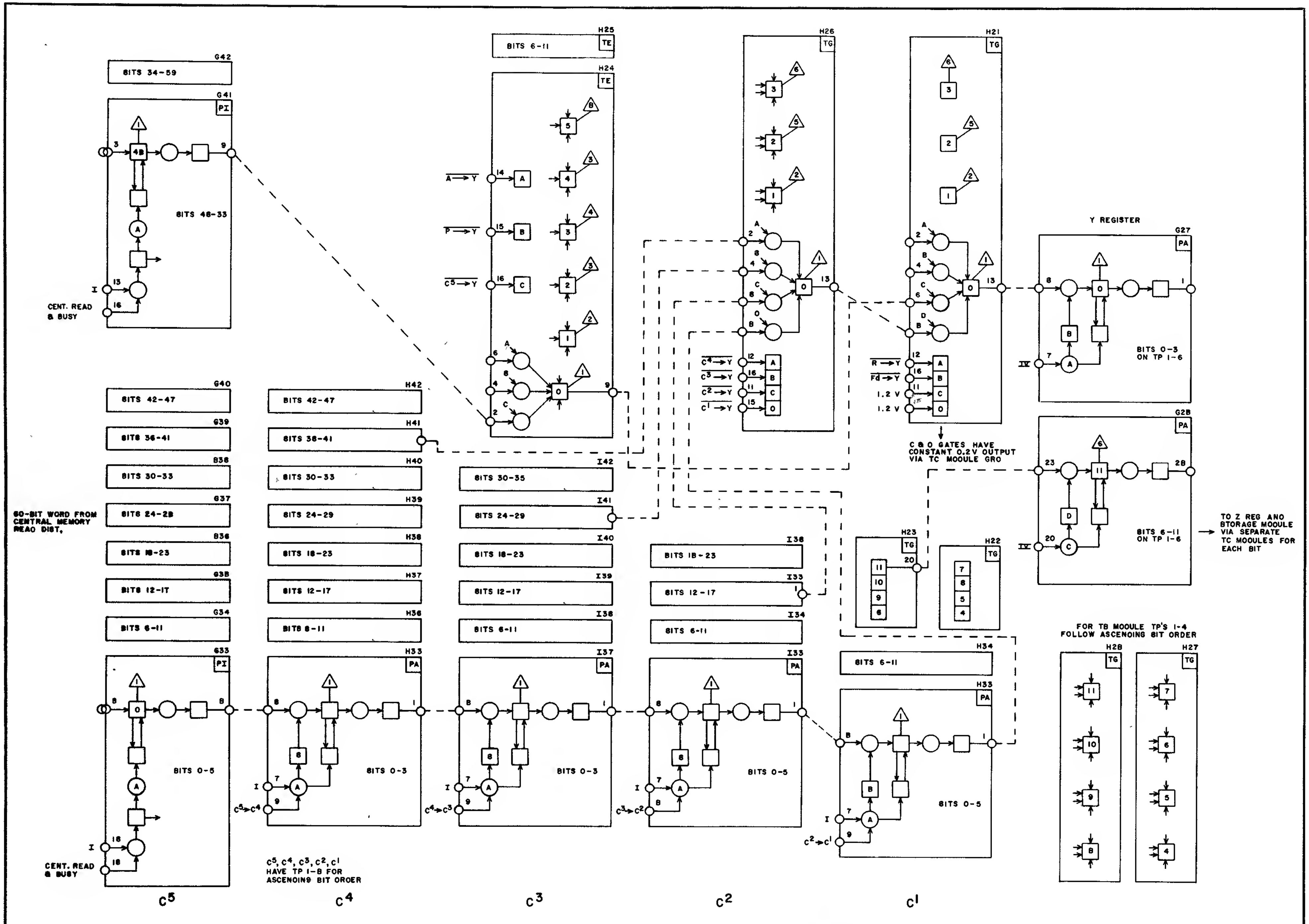


CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR CENTRAL READ CONTROL	PRODUCT 6601 SIZE C	DRAWING NO. 60119300	REV	SHEET 30	53

CENTRAL READ

The Central Read instruction allows a peripheral and control processor to obtain one word (60-bits) or a block of words from Central Memory. The instruction sends a Central Read signal to central address control enabling it to use the 18 bit quantity from A as a central memory address. At the same time, the Central Busy FF is set to inhibit other references to central until the read word is received. When a 60-bit word is sent by central to the Central Read Pyramid, it is accompanied by two control signals; Read Resume which clears the Central Busy FF and a signal which sets the C^5 Full FF. Each rank of the Central Read Pyramid C^1-C^5 has an associated Full/Empty FF used to control the flow of data through the pyramid. C^5 Full and C^4 Empty enables the processor doing the read instruction to send the upper 12 bits of C^5 to memory and the lower 48 bits to C^4. Subsequent steps in the Central Read instruction step the central word down through the pyramid and store the rest of the central word as 12-bit peripheral words. Each step in this storage procedure requires that the next lower rank in the pyramid be empty before a transfer is made. No Central Read instruction may be issued until the C^5 Full FF and Central Busy FF are clear. However, as many as four central memory words, in different stages of disassembly, may be in the Central Read Pyramid at one time. A read instruction for which the proper full and empty conditions are not met must wait until previous instructions progress further and conditions are met.

A 60 instruction reads only one central memory word and stores it as five peripheral words. A 61 instruction reads a block of words specified by (d). In either instruction the first central memory address is specified by (A). For a 60 instruction, d specifies the peripheral address at which the upper 12 bits of the peripheral word are stored; the next lower 12 bits go to d + 1, etc. For a 61 instruction, (d) gives the number of central words to be read and m is the address for the upper 12 bits of the first central word.



CONTROL DATA CORPORATION

COMPUTER DIVISION

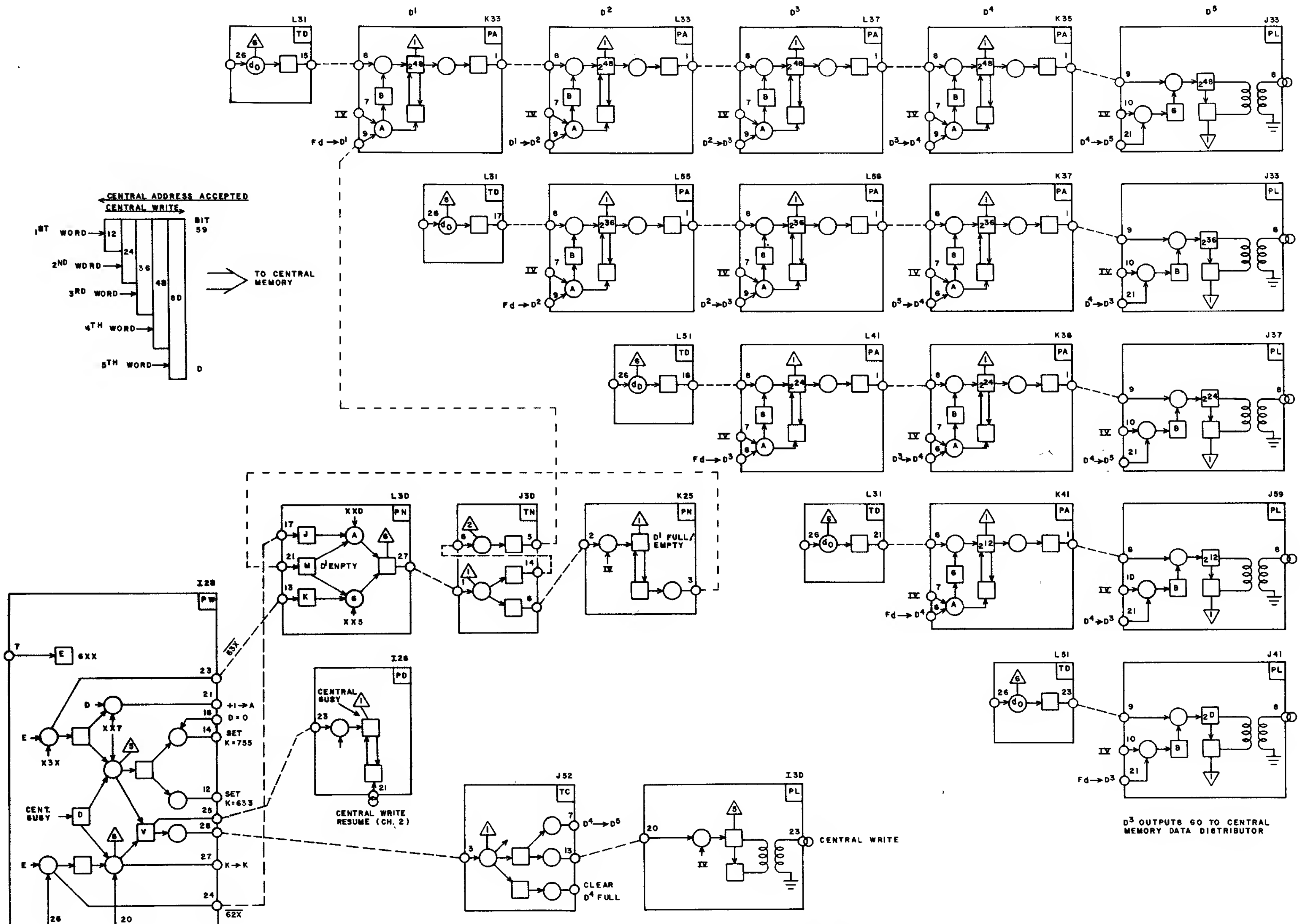
TITLE

PERIPHERAL AND CONTROL PROCESSOR
CENTRAL READ PYRAMID

PRODUCT 6601/04		
SIZE C	DRAWING NO. 60119300	REV B7
SHEET 31		55

CENTRAL WRITE

Central Write instructions send one 60-bit word or a block of 60-bit words to Central Memory. Each 60-bit word sent to Central Memory is assembled in the Central Write Pyramid from five 12-bit peripheral words. A Central Write instruction assembles a 60-bit word and sends the word and a Central Write signal to central address control and sets the Central Busy FF. The Central Write signal enables central address control to accept the 60-bit word and store it at the address specified by (A). When the word has been stored, an accept signal is sent back to clear the Central Busy FF. Up to four Central Write instructions may be in progress at one time with portions of four different words in D^1-D^4. D^5 is an output network only and cannot store a word. The first 12-bit word goes to D^1 and will be the upper 12 bits of the 60-bit word. When a second 12-bit word goes to D^2, D^1 is also sent to D^2. When the fifth word goes to D^5, the 48 bits in D^4 are also sent to D^5 and the 60-bit word is sent to central.



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE PERIPHERAL AND CONTROL PROCESSOR CENTRAL WRITE PYRAMID

PRODUCT	6601/04	
SIZE C	DRAWING NO. 60119300	REV BT
	SHEET 32	57

INPUT/OUTPUT

Each of the 12 independent data channels can handle 12-bit words at a maximum rate of one word every major cycle (equivalent to a 1 megacycle rate). Each channel has an Active/Inactive FF and a Full/Empty FF which indicate channel status to the processors. Any channel may be used by any processor, but the external equipment assigned to a channel is wired in and may be assigned to another channel only by changing cable connections.

The lines of a data channel are:

Input	Output
Data or Status Reply (12 bits)	Data or Function word (12 bits)
Active	Active
Inactive (Disconnect)	Inactive
Full	Full
Empty	Empty
	MC

In addition, two clock signals are available to external equipment: a 1 mc clock and a 10 mc clock. The clock pulses are 25 nsec wide, as are all data and control signals (except master clear). Controllers for each external equipment (or group) perform the conversion between the 6600 pulse signals and the signals required by I/O devices.

A data channel may be used for communication between processors if it is selected for input by one processor and for output by another. The status of data channels may be sensed by instructions 64-67: jump to m if channel d active, etc.

MASTER CLEAR

A Master Clear (MC) signal is generated only by the Dead Start circuit. MC removes all equipment selections (except Dead Start) and sets all channels to the Active and Empty condition (ready for input). MC is a 1 usec pulse which is repeated every 4096 usec while the Dead Start switch is on.

DISCONNECT (75)

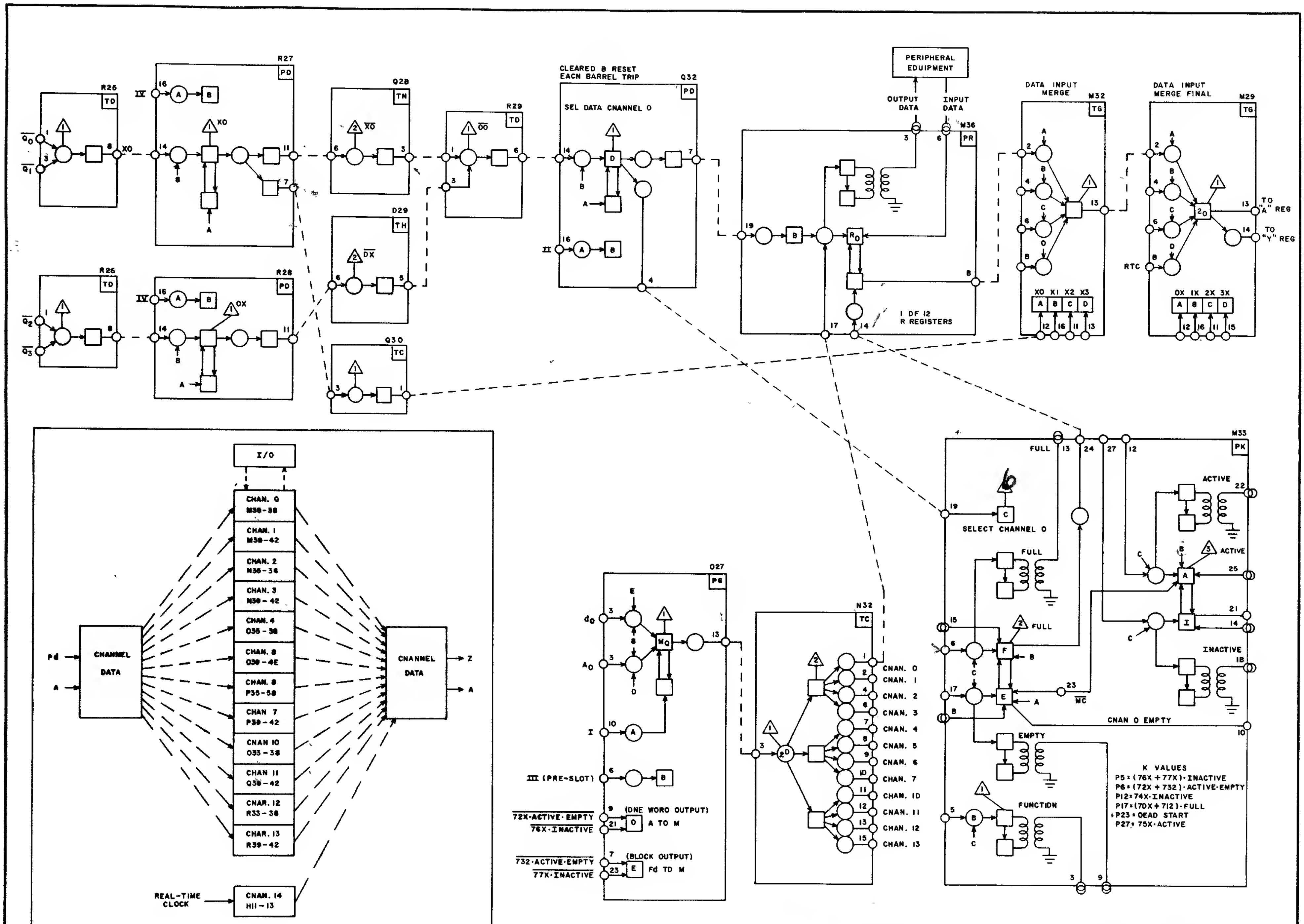
A disconnect instruction clears the channel Active FF if it is set and sends an inactive pulse to the equipment on that channel. If a disconnect instruction is given for a channel which is already inactive, the processor which issued the disconnect will "hang up" and will not be able to continue until the channel is activated by another processor (or by MC).

FUNCTION (76 or 77)

A function instruction sends a 12-bit function code (from A or Fd) on the data lines and sends a Function signal. It also sets the Active and Full FFs for the channel but does not send Active and Full pulses. Upon receipt of the function code, the external equipment sends an Inactive (disconnect) signal, clearing the Active FF in the data channel which in turn clears the Full FF. If a Function instruction is given for an active channel, the processor will hang up until the channel is deactivated.

ACTIVATE (74)

An Activate instruction sends an Active signal on the channel and sets the Active FF if the channel is inactive. If an Activate instruction is given for a channel which is already active, the processor which issued the instruction will "hang up" until the channel is inactivated by another processor or by an Inactive (disconnect) signal from an external equipment on the channel.



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR INPUT / OUTPUT PATHS

PRODUCT: 6601/04

SIZE: C | DRAWING NO. 60119300 | REV: PT

SHEET 33 | 59

DATA INPUT SEQUENCE

An external device sends data to the processor by way of the controller in the following manner:

1 The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidently, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and identifies the word as a function code rather than a data word. The code selects a controller and a mode of operation. Non-selected controllers clear, leaving only the selected one turned on.

2 The controller sends an inactive signal to the processor indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.

3 The processor sets the channel active flag and sends an active signal to the controller which signals the device to start sending data.

4 The device reads a word and then sends the word to the channel register with a full signal which sets the channel full flag.

5 The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word. The device clears its data register and prepares to send the next word.

6 Steps 4 and 5 repeat for each word transferred.

7 At the end of the transfer, the controller clears its active condition and sends an inactive signal to the processor to indicate end of data. The signal clears the channel active flag to disconnect the controller and the processor from the channel.

8 As an alternative, the processor may choose to disconnect from the channel before the device has sent all of its data. The processor does this by dropping the active flag and sending an inactive signal to the controller which immediately clears its active condition and sends no more data, although the device may continue to the end of its data record or cycle (e.g., a magnetic tape unit would continue to end of record and stop in the record gap).

STATUS REQUEST

A status request is a special one word data input transfer in which an external device indicates a ready or error condition to a processor.

1 The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidently, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and defines the word as a function code rather than a data word. The code selects a controller and places it in status mode. Non-selected controllers clear, leaving only the selected one turned on.

2 The controller sends an inactive signal to the processor indicating acceptance of the status function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.

3 The processor sets the channel active flag and sends an active signal to the controller which signals the device to send the status word.

4 The controller sends the status word to the channel register with a full signal which sets the channel full flag.

5 The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word.

6 The processor drops the channel active flag to disconnect the channel and sends an inactive signal to the controller to disconnect it.

DATA OUTPUT SEQUENCE

The processor sends data to an external device in the following manner:

1 The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidently, it sends the word and a function signal to all devices. The function signal tells all controllers to sample the word and identifies the word as a function code rather than a data word. The code selects a controller and a mode of operation. Non-selected controllers clear, leaving only the selected one turned on.

2 The controller sends an inactive signal to the processor, indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.

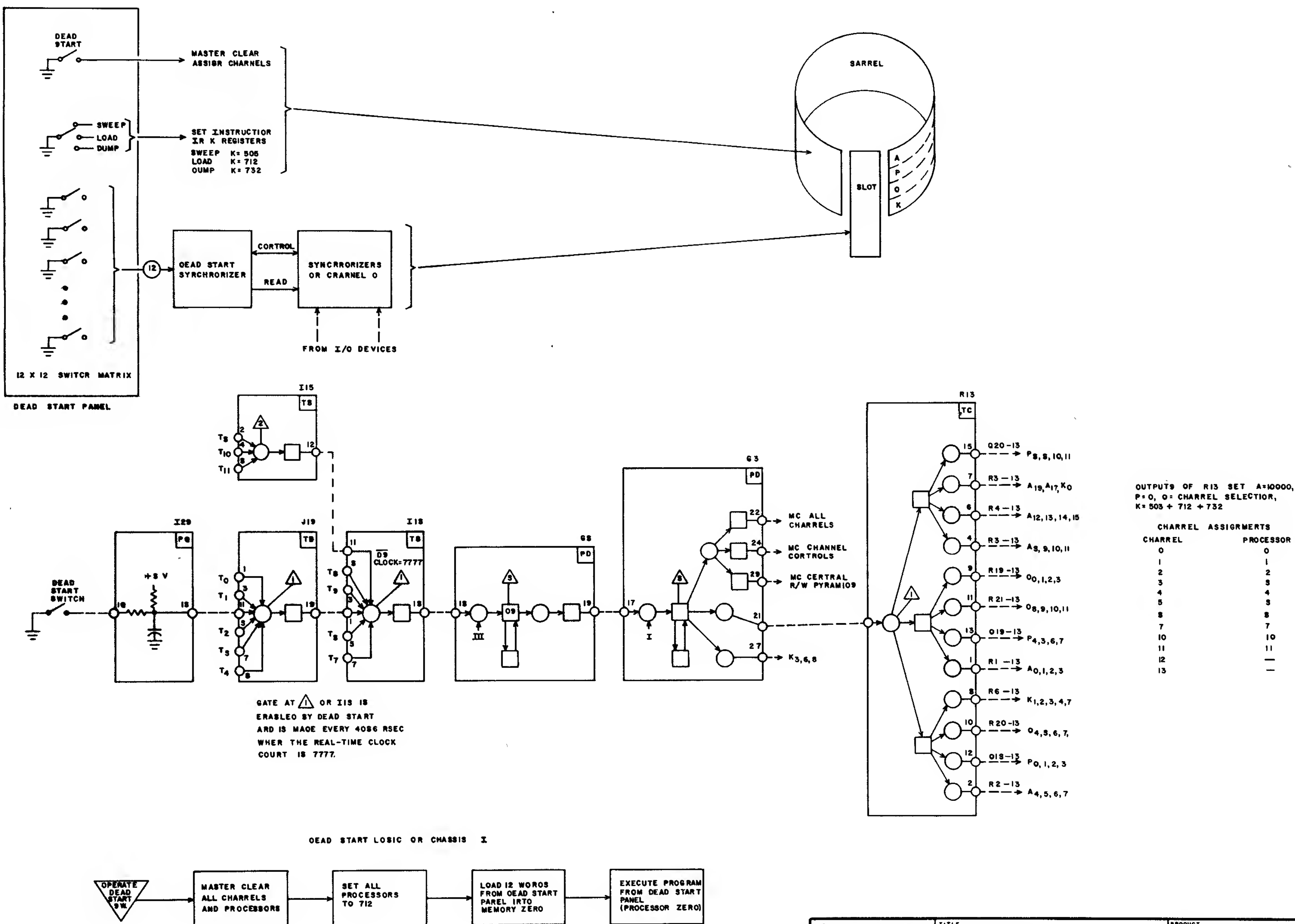
3 The processor sets the channel active flag and sends an active signal to the controller which signals the device that data flow is starting.

4 The processor places a data word in the channel register and sets the full flag. Coincidently, it sends the word and a full signal to the controller.

5 The controller accepts the word and sends an empty signal to the processor where it clears the channel register and drops the full flag.

6 Steps 4 and 5 repeat for each processor word.

7 After the last word is transferred and acknowledged by the controller empty signal, the processor drops the channel active signal to the controller to turn it off.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: PERIPHERAL AND CONTROL PROCESSOR DEAD START

PRODUCT: 6601/04

SIZE: C | DRAWING NO. 60119300 | REV BT

SHEET 34 | 61

DEAD START

Dead Start is a system used to initially start the computer, dump the contents of the peripheral and control processor memories to a printer or other output device, or sweep memory without executing instructions.

The Dead Start panel contains a 12x12 matrix of toggle switches, a Sweep-Load-Dump switch and a Dead Start switch. It also contains memory margin switches which are used for maintenance checks.

LOAD

To initially load programs and date, the Sweep-Load-Dump switch is put in the Load position. The matrix of toggle switches is set to a 12-word program (up = "1", down = "0"). When the Dead Start switch is turned on, a 1 usec Dead Start pulse:

1 Assigns to each peripheral and control processor the corresponding I/O channel.

2 Sets all channels to Active and Empty

3 Sets K for all processors to 712 (Input)

4 Sends a MC on all channels

5 Sets P for all processors to zero. (A is then set to 10000_8 in the barrel)

The Dead Start pulse is repeated every 4096usec while the Dead Start switch is on. To start the machine, the DS switch is normally turned on momentarily, then off. Recycling of the DS pulse is controlled by the Real Time Clock; the pulse is formed by ANDing DS switch in the ON position with 10 bits of Real Time Clock.

When the Dead Start controller on channel 0 receives the MC sent by Dead Start, it sends a Full pulse but no data. When processor 0 receives the Full, it stores the content of the channel 0 input register (All zeros) in location 0000 and sends an Empty pulse to the Dead Start controller. The Dead Start controller then acts like an input device, sending twelve 12-bit words from the switch matrix which processor 0 stores in locations $0001\text{-}0014_8$. After the last word, the Dead Start controller sends a disconnect which causes processor 0 to exit from the 712 instruction. Processor 0 reads location 0000, adds one to its contents and goes to 0001 for its next instruction. It then executes the 12-word (or less) program which normally is a control program to load information and begin operation. The other processors are still set to 712 (waiting to input when their channels become full) and may receive data from processor 0 via their assigned I/O channels.

SWEEP

If the DS switch is operated with the Sweep-Load-Dump switch in the Sweep position, all processors are set to a 505 instruction and P registers set to 0000. Since the 50 instruction doesn't require 5 trips around the barrel there is no logic to clear or advance K from 505. The 50X translation of K, causes all processors to sweep through their memories; reading and restoring without executing instructions. This is a maintenance routine and may be used to check the operation of memory logic.

DUMP

Dead Start with the Sweep-Load-Dump switch in the Dump position:

1 Sets all processors to 732.

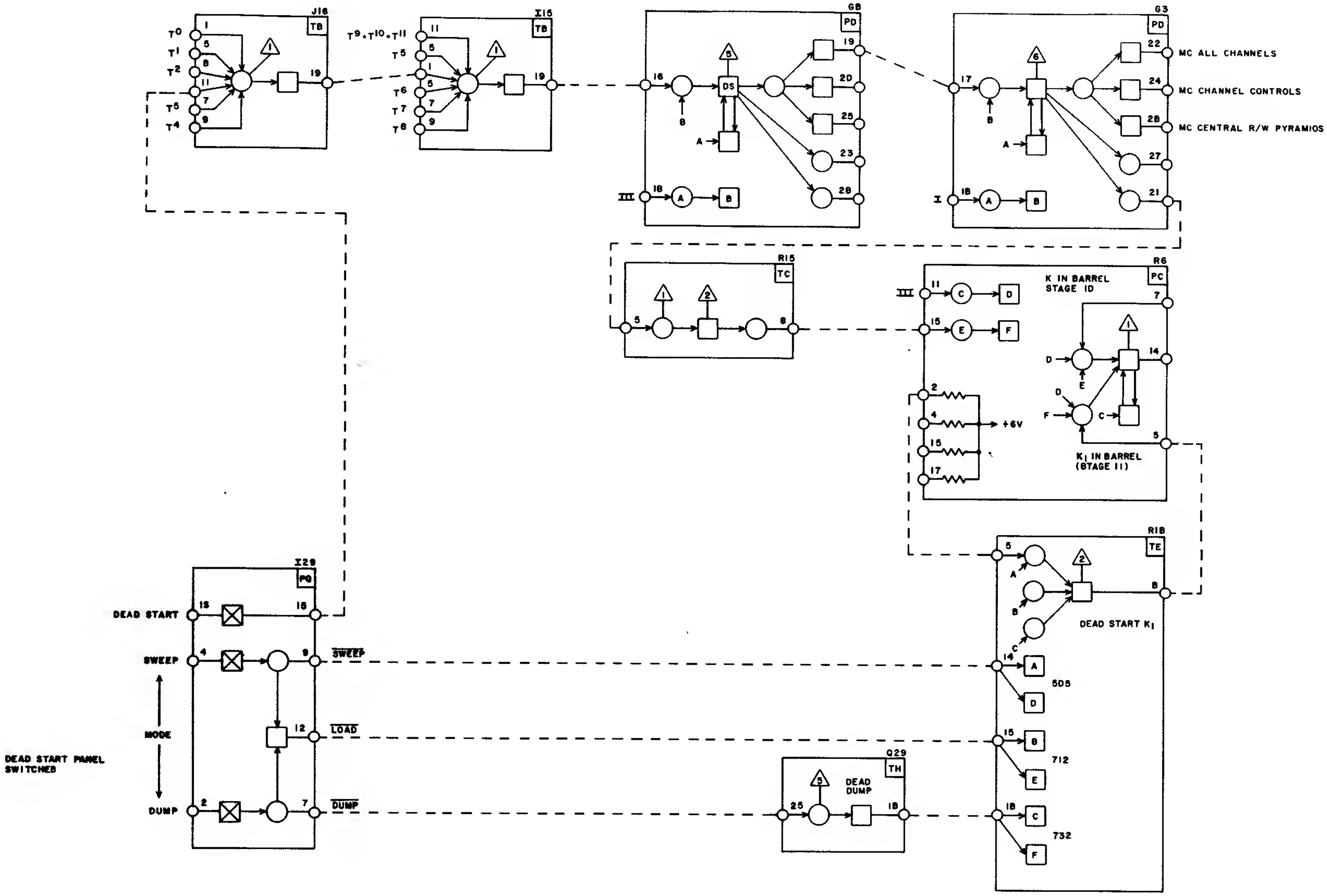
2 Sends MC on all channels.

3 Holds channel 0 Active and Empty.

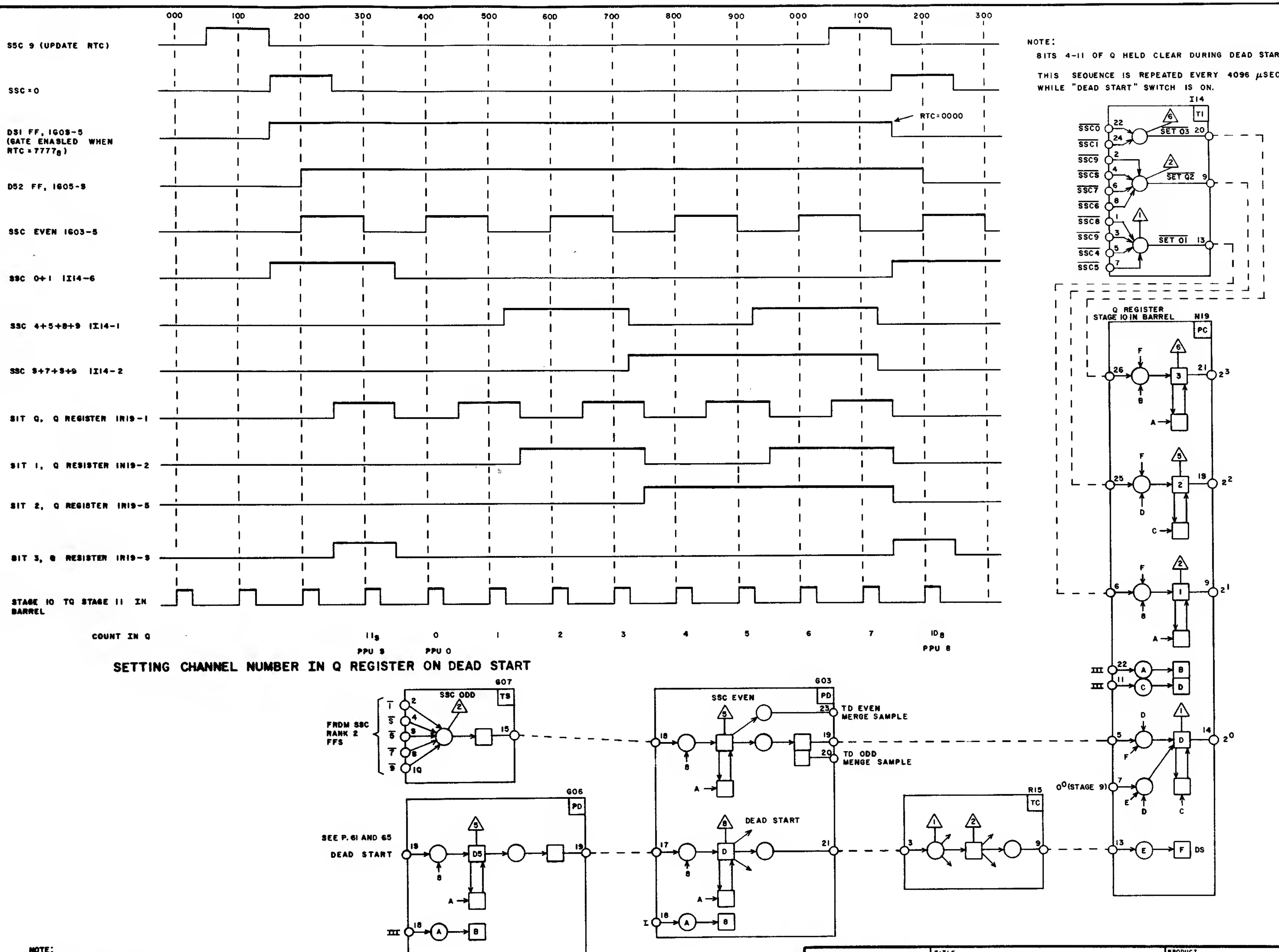
4 Assigns each processor to its corresponding I/O channel.

5 Sets all A and P registers to 0.

All processors sense the Empty and Active condition of their assigned channels, output the content of their address 0000, set their I/O channels to Full, and wait for an Empty. All processors advance P by one and reduce A by one ($A = 7776_8$). Channel 0, which is assigned to processor 0, is held by Empty by the Dump switch. Processor 0 therefore cycles through the 732 instruction until A = 1 and then goes to memory location 0001 for its next instruction. Processor 0 has sent its entire memory content on channel 0 although no I/O device was selected to receive it. Processor 0 is now free to execute a dump program which must have been previously stored in memory 0 (beginning at location 0001).



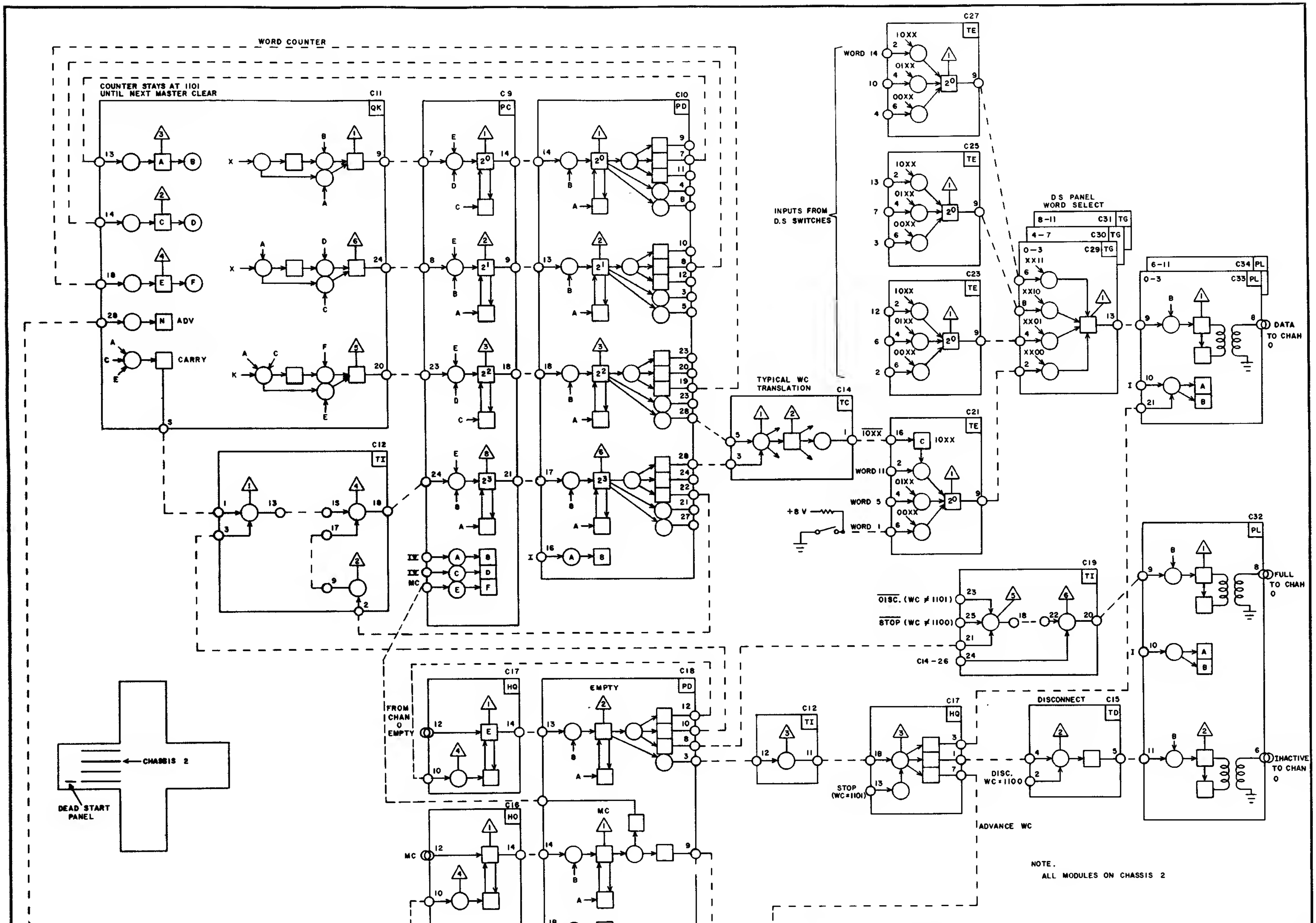
CONTROL DATA CORPORATION	TITLE PERIPHERAL AND CONTROL PROCESSOR	PRODUCT 6601/04	
		SIZE C	DRAWING NO. 60119300 / REV K
COMPUTER DIVISION	712, 732, 505→K (DEAD START)	SHEET 35	63



SETTING CHANNEL NUMBER IN Q REGISTER ON DEAD START

NOTE:
RTC = REAL TIME CLOCK
SSC = STORAGE SEQUENCE CONTROL

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR SET Q, DEAD START	PRODUCT 6601/04 SIZE C DRAWING NO 60119300 REV BT SHEET 36 65



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR DEAD START CONTROLLER	PRODUCT 6601/04/13/14 SIZE C · DRAWING NO. 60119300 · REV BT SHEET 37 · 67

CENTRAL MEMORY (131 K)
CONTENTS

Pub. No. 60119300

Rev. M

ADDRESSING

The CP programs are stored in CM, and all PPs may use CM for supplementary storage or inter-communication control. Thus CM addresses are generated by the CP and all PPs.

Each processor sends a CM address to a common address clearing house, or stunt box, from where they are sent on to CM. The stunt box can accept addresses from the several sources at 100-nsec intervals (maximum rate) on a priority basis and in turn issue one address every 100 nsec to CM.

An address goes to all banks of CM for decoding, and the referenced bank returns an accept signal to the stunt box if the bank is not busy (free) with a previous reference. The stunt box saves each address that it sends to CM in a hopper mechanism, and, if the address is not accepted, it is recovered from the hopper and re-issued to CM and again saved. The issue-save cycle repeats until an accept is received to void the hopper address. Up to three addresses can be saved in the hopper. However, an address is always accepted within 2000 nsec (worst case because of bank conflict) of the first time it is issued.

DATA DISTRIBUTION

Data to and from CM is distributed from a data distributor. The word from a read reference goes from CM to the data distributor and then to the requesting processor. A word to be stored during a write reference goes from the processor to the data distributor to CM. The distributor can transfer a word to or from CM every 100 nsec. A store word goes to all banks of CM, but separate storage control mechanisms for each bank insure that the word is stored in the proper bank.

The distributor routes data to and from proper origins and destinations as directed by control information or tags received from the stunt box. The tags are entered in the stunt box along with each address and serve to identify the address sender, origin or destination of data, and nature of the address, e.g., read, write, or PP exchange jump. The stunt box sends the tags to the data distributor (and to destinations in the processors for read references) when an address is accepted, and the distributor accomplishes the data transmission. For write references, the data source sends the word to the distributor, where it is held temporarily before it is stored.

STORAGE

The many banks of storage in CM are evenly distributed on 8 chassis in the computer. There are four banks per chassis.

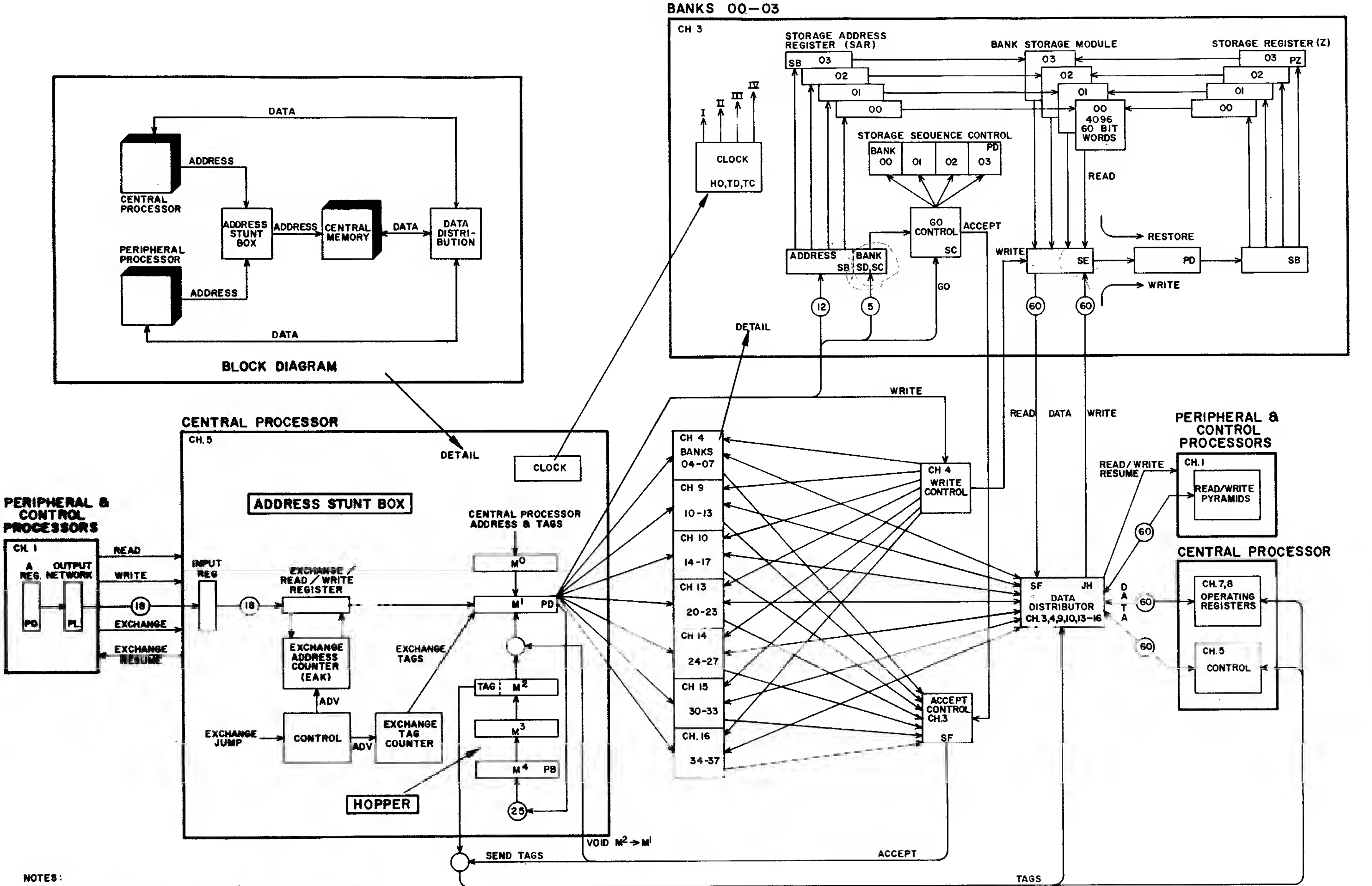
The circuit organization allows the four banks to operate independently and be phased into operation at 100-nsec intervals, which corresponds to the maximum rate at which the stunt box issues addresses. A chassis input register receives the 17-bit address from the stunt box and distributes the 12-bit address to 1 of 4 storage address registers associated with the four banks. Hence 32 consecutive addresses referencing 32 separate banks may be accepted at 32 consecutive minor cycle intervals and result in a data word flowing to or from CM in 32 consecutive minor cycle intervals. The independent controls for each bank and treatment of the address and data word insure that only one bank is in a given time segment of its 1000 nsec storage cycle at any one time. At least one minor cycle separates the storage cycle of all banks.

A word read from any bank is sent to a common temporary storage register and to the data distributor by a common path. A word to be restored is then sent to a write register by way of a buffer register. The write register sends the word to 1 or 4 restoration registers for restoring in the proper bank.

A word from the data distributor during a write reference goes to the temporary storage register on all chassis and then follows the restore path for writing in memory. Only one of the many banks is in the proper time spot in its storage cycle to store the word received, and this bank is the one associated with the write address.

A go signal with each address from the stunt box allows a group of four banks (one chassis) to recognize and translate the bank bits. The referenced bank, if not busy, sends an accept to the stunt box and starts 1 of 4 storage sequence control circuits, which in turn direct the 1000 nsec storage cycle for the selected address.

A write signal may also accompany each address from the stunt box. It distinguishes read and write references and controls the path to the restoration registers. The CM uses the same 12-bit storage module as used in the PPs, but five are driven in parallel to hold the 60-bit word.



NOTES:

1. ADDRESSES SENT TO CM FROM M^1 AT MINOR CYCLE RATE.
2. DATA MOVES TO/FROM CM AT MINOR CYCLE RATE.
3. ADDRESS TAGS DEFINE ORIGIN / DESTINATION OF DATA.
4. TIME FROM $M^1 \rightarrow$ CM TO RESPONSE TO CM ACCEPT IS 200 nSEC
   a. M^1 STORED IN M^4 AT ISSUE TIME AND MOVES TO M^2 IN TIME SEQUENCE.
   b. ACCEPT VOIDS RE-ISSUE OF ADDRESS FROM HOPPER.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY ADDRESS - DATA FLOW	PRODUCT 6601 SIZE C · DRAWING NO. 60119300 · SHEET 38	REV K 1

A go control circuit is associated with each chassis (four banks) of CM. The circuit has several functions.

1. Recognize an address from the stunt box and determine if it is located in an associated bank.
2. Sends an accept to the stunt box if the address is valid and the bank is free.
3. Starts the 1000 nsec storage cycle to read or store the word at the selected address.

No accept is sent to the stunt box if the selected bank is executing a storage cycle from a previously issued address (bank busy case). The address is ignored in this case. The time of address issue from the stunt box and the time the accept should be received back at the stunt box is 200 nsec, and this time is used by the stunt box to determine if the address has been accepted. An accept at the proper time voids reissue of the address; otherwise address reissue continues until the accept is received.

BANK SELECTION

The go signal accompanying each address signals all CM go control circuits to search the bank selection bits and determine if the 12-bit address is located in one of its associated banks. A translator circuit in each go control translates the lower five bits of the address, stores the selection in a FF (one FF for each bank), sends the accept, and starts the storage sequence control circuit to start the storage cycle.

The five bits provide 32 unique codes, one for each bank. The upper three bits select 1 of 8 chassis and the lower two bits 1 of 4 banks on the chassis.

The 17-bit address and bank quantity is stored in an input FF register. Before an address is received, a clock pulse presets the upper three of the five bank bits to the complement of the quantity it should recognize. Thus, for a zero chassis selection (physical chassis 3), the upper three bits are preset to 111XX, the complement of 000XX. A 000XX bank code then is necessary to complete the go FF output gate, which in turn allows recognition of the lower two bits of the bank selection.

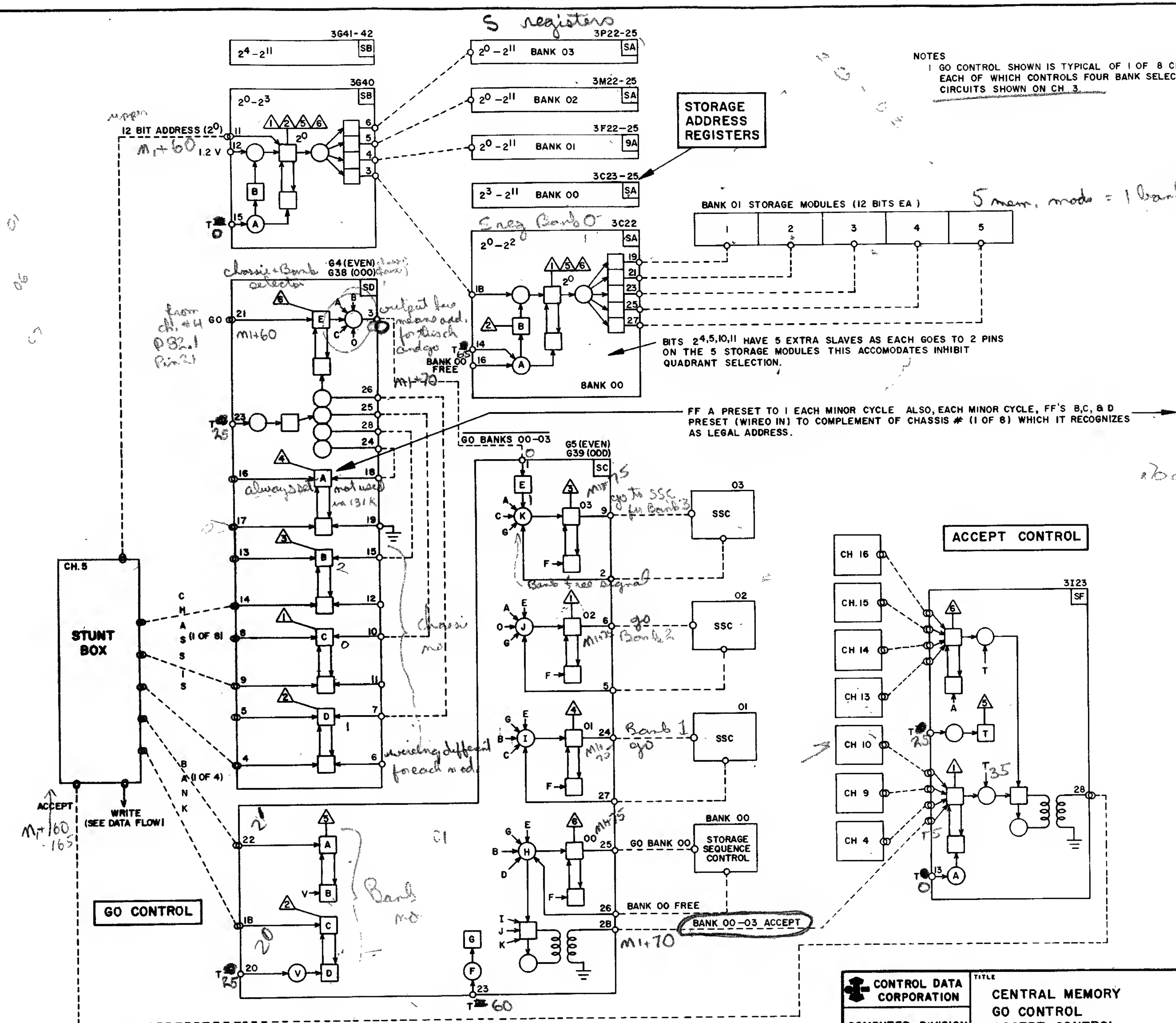
Four unique translations are made from the lower two bits of the bank selection bits and stored in separate FFs. A go from the 1 of 8 translator, a bank free condition from the storage sequence control circuit, and a clock pulse gates the 1 of 4 storage and turns on the accept signal. The set FF then starts an associated storage sequence control circuit.

ACCEPT CONTROL

The accept signal indicates a bank is free and has accepted the address in its chassis input register. The time interval from address issue from the stunt box to receipt of the accept in the stunt box allows the stunt box to determine if the address has been accepted. If so, the address in the stunt box hopper is destroyed, and address tags are sent from the stunt box to the data distributor and other areas to tell the address sender to send its data word (write reference) or be ready for receipt of the word read (read reference).

One accept is associated with each chassis for a maximum of eight signals. All are combined in a common OR circuit which feeds the stunt box. Since an address may be sent each 100 nsecs, an accept may be sent to the stunt box every 100 nsecs, with each accept delayed from its associated address by 200 nsecs.

NOTES
1. GO CONTROL SHOWN IS TYPICAL OF 1 OF 8 CIRCUITS EACH OF WHICH CONTROLS FOUR BANK SELECT CIRCUITS CIRCUITS SHOWN ON CH 3.



LOGICAL SELECTION	CHASSIS NO. SELECTION
0	3
1	4
2	9
3	10
4	13
5	14
6	15
7	16

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: CENTRAL MEMORY GO CONTROL ACCEPT CONTROL

PRODUCT 6601 | SIZE C | DRAWING NO. 60119300 | REV K | SHEET 39 | 3

STORAGE SEQUENCE CONTROL

Storage sequence control responds to a bank go condition from go control and generates a series of timing signals which direct the basic cycle of the storage module. In general, the circuit establishes the bank free condition, makes the address available to the storage module, and then issues read, sense, start and end inhibit, bank merge, and write drive signals to sequence reading and writing. The sense signal samples the differential amplifier which receives the data word read out on the double-ended sense lines from storage. The signals time the basic pulse sequence of the 1000 nsec storage cycle. The storage module discussion details the circuits which respond to the address and read and write drive signals, and thereby make the read word available on the sense lines, or store the word to be written or restored in memory.

TIMING CHAIN

The timing chain is a series chain of FFs whose outputs drive slave inverters, which in turn supply the various signals to sequence reading and writing in CM. A pulse enters the chain and is transferred to successive FFs at 50 nsec intervals. A bank go signal sets the read FF to start the sequence. Each FF is set for 400 nsecs; slave inverters from set and cleared FFs in the chain are combined to establish timed gating signals for the various drive signals.

BANK FREE

The bank free condition is established when all FFs in the chain are cleared, i. e., no pulse is travelling down the chain. The read FF, and intermediate FF, and write FFs (last FF in chain), contribute timing signals to the bank free circuit and indicate whether a pulse is in the chain. All three FFs must be cleared to signal bank free, but their set states overlap to signal bank busy when a pulse is in the chain.

The bank free signal allows go control to respond to its back translation circuits and issue a bank go signal which sets the read FF to turn off the bank free signal.

STORAGE CYCLE TIMING

The following are the recommended times or timing durations for Central Memory in all 6000 series computers:

Strobe (time 75 ± 5 nsec)

This is measured on TP5 of the SE module, (see page 8. 1). This time should be adjusted by varying the length of wire to pin 16 of the SG module.

Read-On(255 nsec ± 5 nsec) before Strobe.

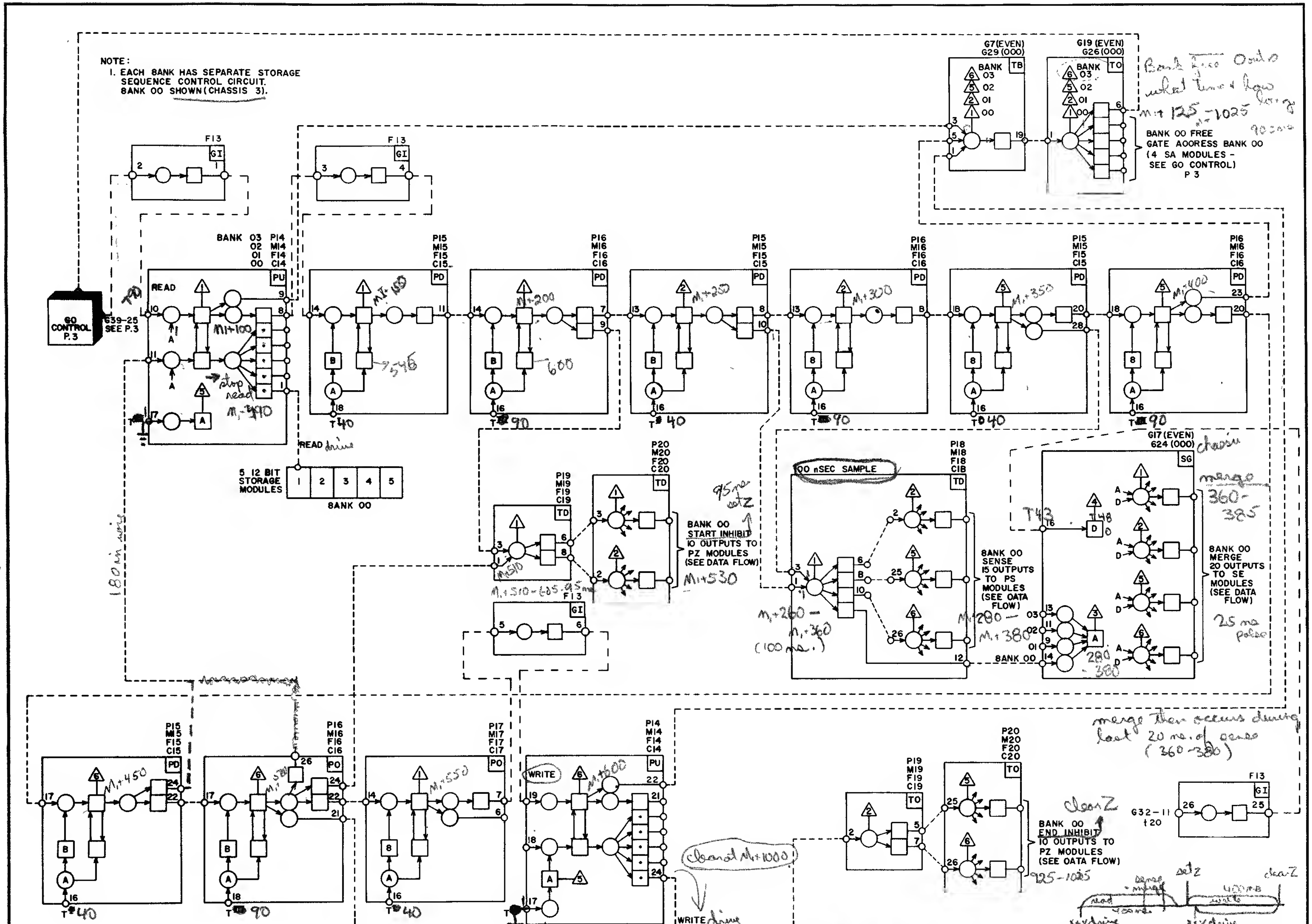
This is measured on pin 1 of the PU module. This time should ba adjusted by varying the length of wire to pin 10 of the PU module and/or pin 2 of the GI module.

Read-Off (395 nsec ± 5 nsec) after the start of Read

This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 11 of the PU module.

Write (355 nsec ± 5 nsec)

This is measured on pin 24 of the PU module. This time should be adjusted by varying the length of wire to pin 19 of the PU module and/or pin 5 of the GI module. See also page 8. 1.



CONTROL DATA CORPORATION	TITLE	PRODUCT 6601	
COMPUTER DIVISION	CENTRAL MEMORY STORAGE SEQUENCE CONTROL	SIZE C / DRAWING NO. 60119300	REV BT
		SHEET 40	5

DATA FLOW

In a read reference, the read word from the specified address flows from the storage modules to the data distributor and also back to the storage modules for restoration. The SE modules send the read word to the distributor and start the restore portion of the cycle. The restore FFs on these modules are cleared just before receiving the read word.

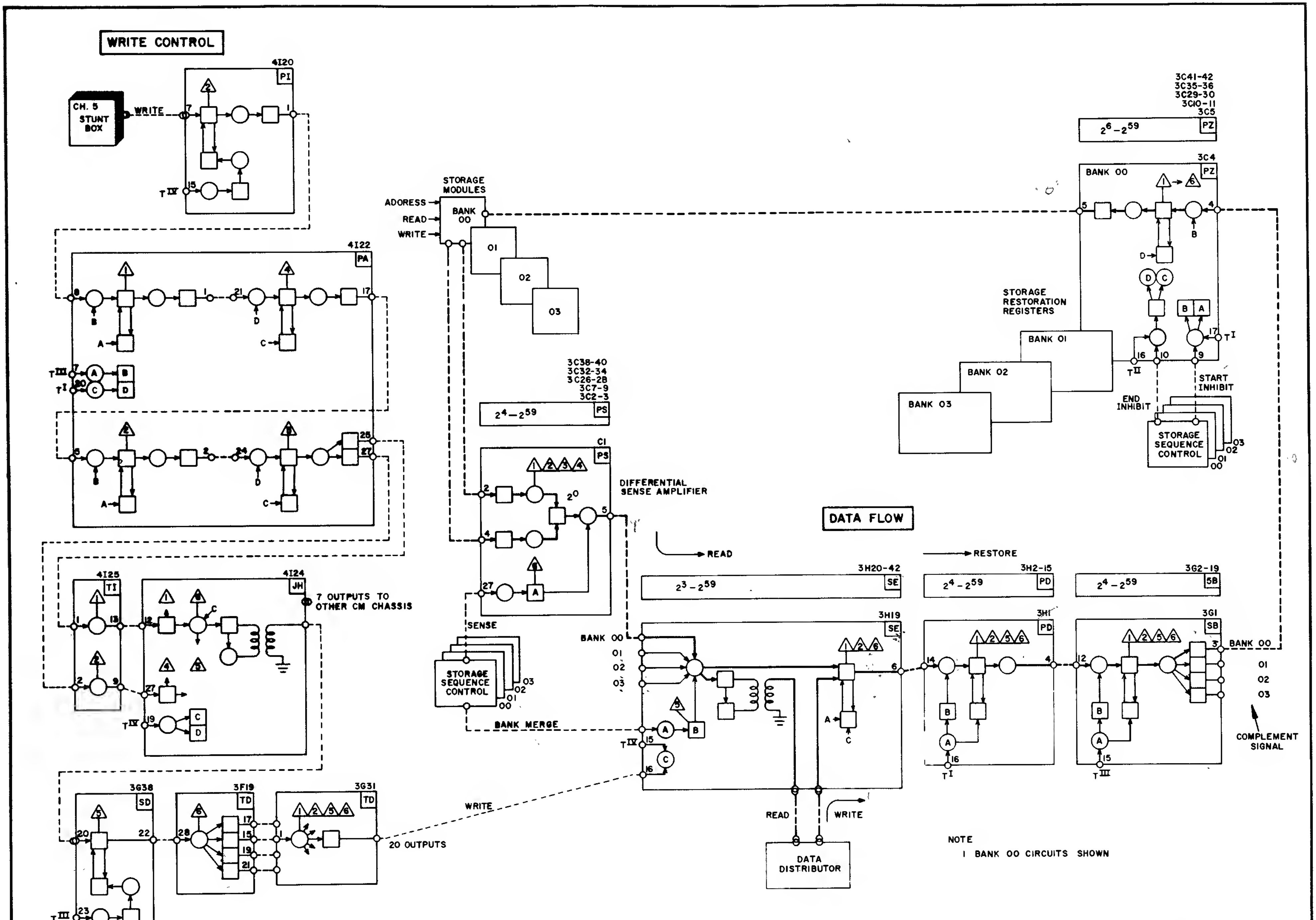
In a write reference, the read word from the specified address is sent to the data distributor and entered in the restore FFs of the SE modules. The restore FFs are cleared again to destroy the read word and reset with the write word which is stored in place of the read word during its normal restore cycle. The write control circuit and timing of stunt box tags direct the sequence.

WRITE CONTROL

Write control clears the restore FFs in the SE modules when writing in memory and thereby allows entry of the write word into the restore circuits.

A write signal from the stunt box enters the write control timing chain at the same time as the memory address is received in the input register of all memory chassis. The timing chain feeds a pulse to all chassis where they are fanned out and clear the restore FFs on the respective chassis SE modules. The delay time through the chain and format just exceeds the read access time and thereby destroys the read word immediately after it enters the SE restore FF. Effectively, the pulse in the timing chain runs in parallel with the pulse in the storage sequence control associated with the selected bank, but the write pulse from the timing chain fanout is emitted just after the bank merge pulse (which enters the read word in the SE restore FFs) from storage sequence control. Write pulses may enter the chain at minor cycle intervals and each is associated with a parallel operating storage sequence control.

The timing within the data distributor is such that a write word is sent to the SE modules slightly later than the SE modules send the read word to the data distributor.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY DATA FLOW, WRITE CONTROL SERIALS 1-7	PRODUCT 6601 SIZE C · DRAWING NO. 60119300 · REV R	SHEET 41 · 7

DATA DISTRIBUTOR

The data distributor distributes read and write words to and from CM. Read words are sent to CP control on chassis 5, CP registers on chassis 7 and 8, and to the PP on chassis 1.

Write words are accepted from CP control on chassis 5 (exchange jump or return jump instructions), CP register chassis 7 and 8 (X^{0-7} registers), or from the PP on chassis 1.

Address tags from the CP stunt box define the read or write cases and the origin or destination of the data.

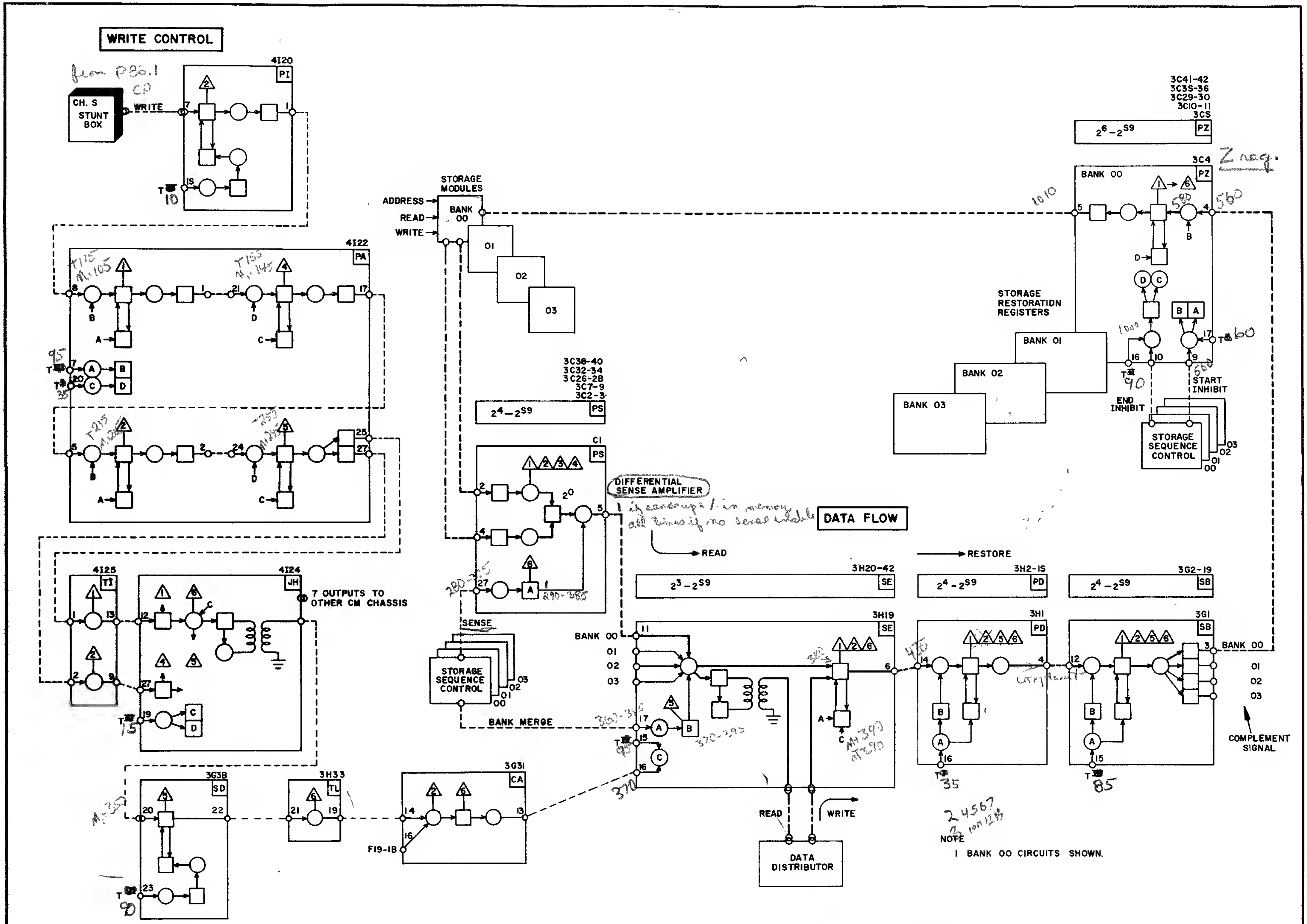
STORAGE CYCLE TIMING

Inhibit On and Off

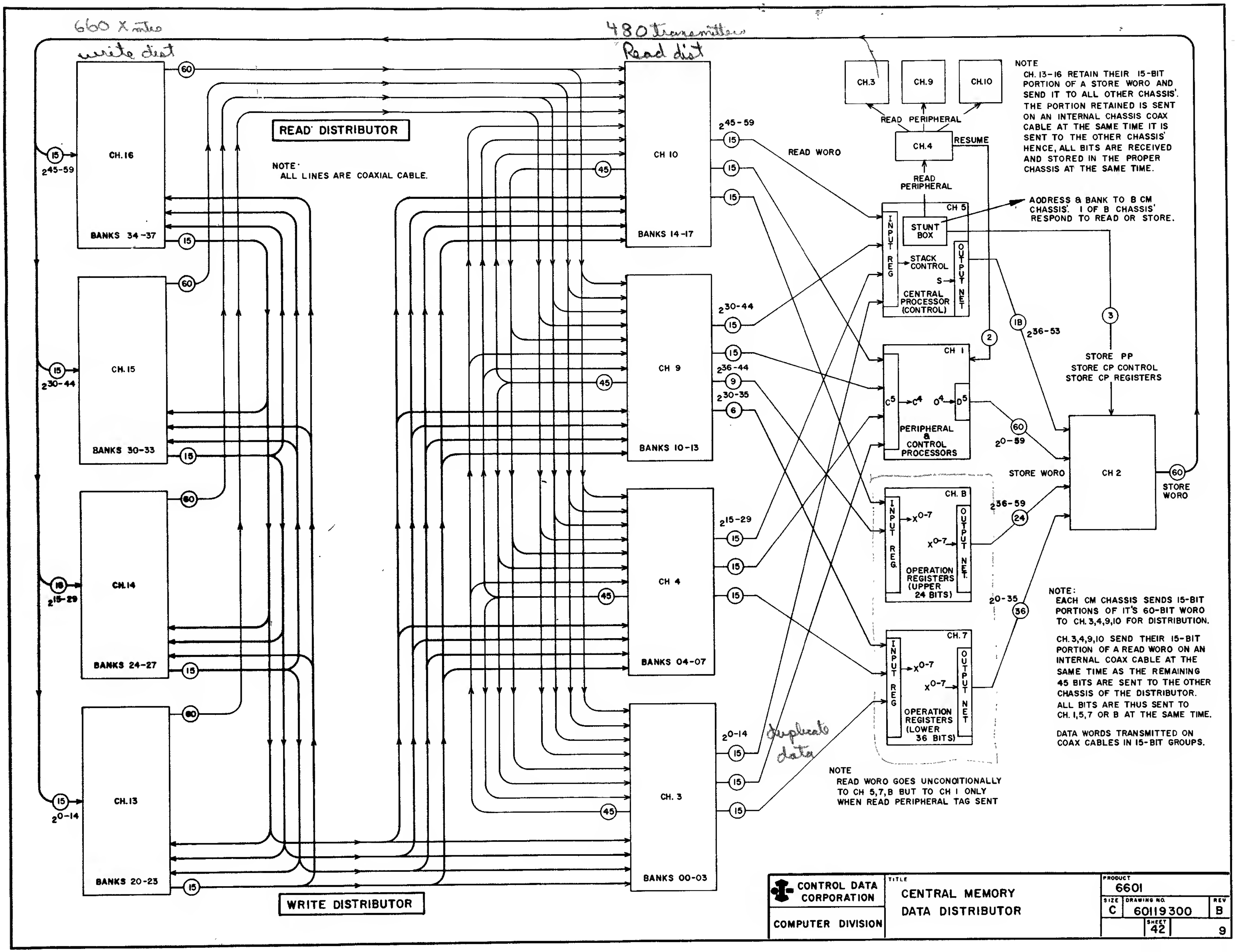
The inhibit should turn on at least 20 nsec before the start of the Write, and stay on at least 15 nsec after the end of the Write. The inhibit time is measured on pin 5 of the PZ module and is compared to the Write on pin 24 of the PU module. It should not be necessary to adjust the on time for the inhibit 30-50 nsec is the usual delay between inhibit-on and write-on. The off time is adjusted by varying the length of wire to pin 14 of C21, F21, M21, or P21 (clock working ranks).

All of the preceding times are measured from the first crossing of the half amplitude point of the waveform. It is necessary that Change Order 14965 (6600) or 15349 (6400 and 6500) are installed prior to making any of the timing adjustments.

Use the SC module (test points 6, 4, 1, 3 for banks 0, 1, 2, 3) for the trigger source. It may not be possible to obtain a 395 nsec duration pulse for the read using the 180" wire called out in Change Order 14965 (6600 only). An additional change order has been written with a retrofit on failure. This change order just clears the read portion of the PU from a later time in the Storage Control Sequence. Change Order 17014 is applicable only to the 6600. The retrofit case changes the 180" wire from pin 24 of C15, F15, M15 or P15, to pin 26 of C16, F16, M16 or P16. The wire is then cut to the correct length to obtain 395 nsec $\pm$ 5 nsec.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY DATA FLOW, WRITE CONTROL SERIALS 8-UP ONLY	PRODUCT 6601/13 SIZE C · DRAWING NO. 60119300 · REV BT SHEET 271 · 8.1


660 X mitrs
write dist
480 transmitters
Read dist
READ DISTRIBUTOR
NOTE:
ALL LINES ARE COAXIAL CABLE.
WRITE DISTRIBUTOR
CH.16
BANKS 34-37
CH.15
BANKS 30-33
CH.14
BANKS 24-27
CH.13
BANKS 20-23
CH 10
BANKS 14-17
CH 9
BANKS 10-13
CH 4
BANKS 04-07
CH. 3
BANKS 00-03
CH.3
CH.9
CH.10
READ PERIPHERAL
CH.4
RESUME
READ PERIPHERAL
READ WORD
CH 5
INPUT REG
STUNT BOX
STACK CONTROL
OUTPUT NET
CENTRAL PROCESSOR (CONTROL)
CH 1
PERIPHERAL & CONTROL PROCESSORS
CH. B
OPERATION REGISTERS (UPPER 24 BITS)
CH. 7
OPERATION REGISTERS (LOWER 36 BITS)
CH 2
STORE WORD
STORE PP
STORE CP CONTROL
STORE CP REGISTERS
ADDRESS & BANK TO 8 CM CHASSIS. 1 OF 8 CHASSIS RESPOND TO READ OR STORE.
duplicate data
NOTE
CH. 13-16 RETAIN THEIR 15-BIT PORTION OF A STORE WORD AND SEND IT TO ALL OTHER CHASSIS. THE PORTION RETAINED IS SENT ON AN INTERNAL CHASSIS COAX CABLE AT THE SAME TIME IT IS SENT TO THE OTHER CHASSIS. HENCE, ALL BITS ARE RECEIVED AND STORED IN THE PROPER CHASSIS AT THE SAME TIME.
NOTE:
EACH CM CHASSIS SENDS 15-BIT PORTIONS OF IT'S 60-BIT WORD TO CH. 3,4,9,10 FOR DISTRIBUTION.
CH. 3,4,9,10 SEND THEIR 15-BIT PORTION OF A READ WORD ON AN INTERNAL COAX CABLE AT THE SAME TIME AS THE REMAINING 45 BITS ARE SENT TO THE OTHER CHASSIS OF THE DISTRIBUTOR. ALL BITS ARE THUS SENT TO CH. 1,5,7 OR B AT THE SAME TIME.
DATA WORDS TRANSMITTED ON COAX CABLES IN 15-BIT GROUPS.
NOTE
READ WORD GOES UNCONDITIONALLY TO CH 5,7,B BUT TO CH 1 ONLY WHEN READ PERIPHERAL TAG SENT
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY DATA DISTRIBUTOR
PRODUCT 6601
SIZE C
DRAWING NO. 60119300
REV B
SHEET 42
9

The read distributor accepts read words from the 8 CM chassis and routes them to the several destinations.

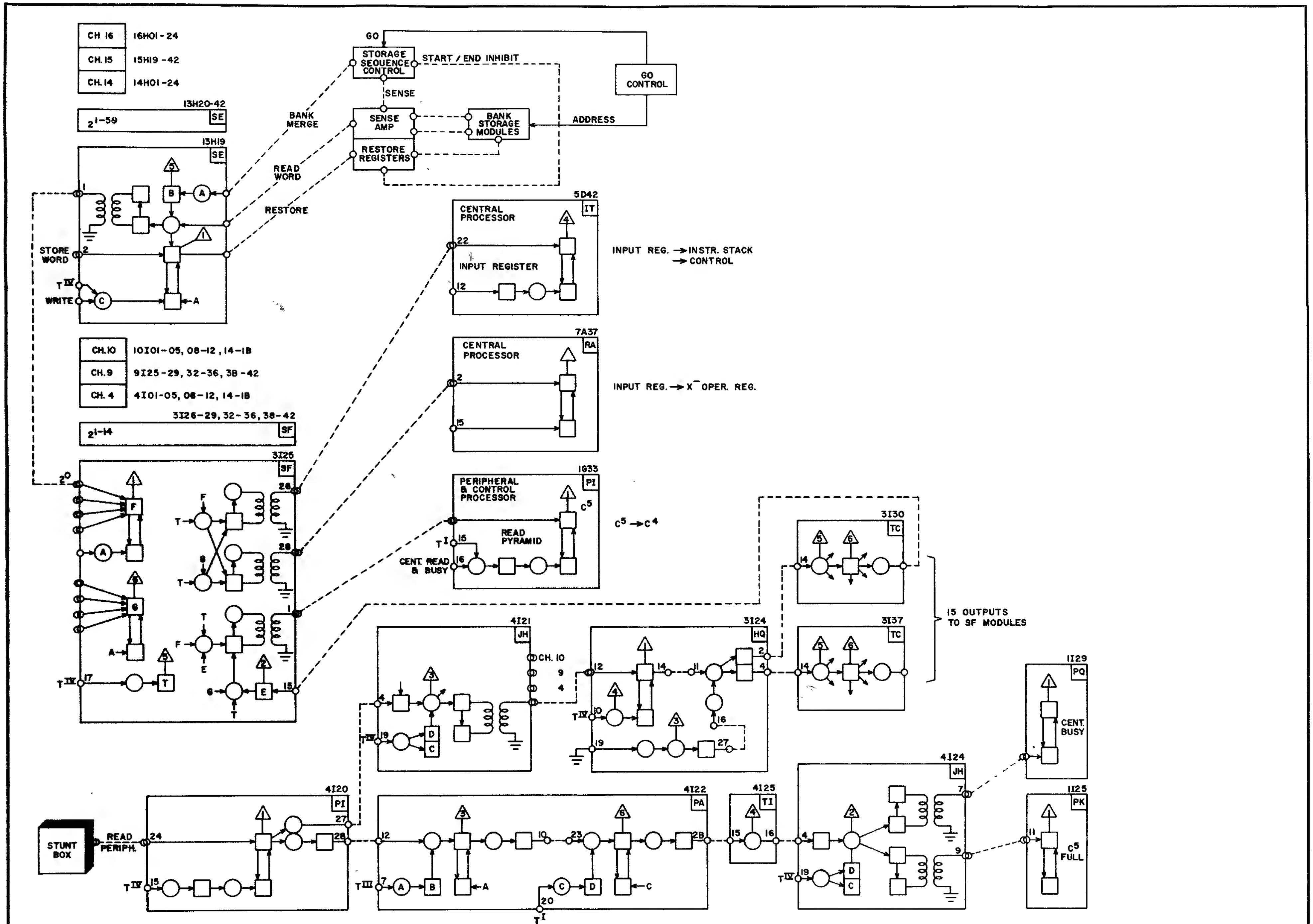
The distributor is organized on chassis 3, 4, 9, and 10, each of which handles 15 bits of the 60-bit word. Chassis cable limitations dictate the organization. The listing below shows the bits handled by each chassis.

CHASSIS	BITS
3	0-14
4	15-29
9	30-44
10	45-59

Chassis 13-16 each send the same 15-bit group to chassis 3, 4, 9, and 10. A read word from chassis 3 retains bits 0-14 but sends remaining bits in three groups to chassis 4, 9, and 10. Read words from chassis 4, 9, and 10 are handled similarly. Intra-chassis coaxial cables are used on chassis 3, 4, 9, and 10 for their 15-bit portions so that timing is consistent with the chassis receiving the data.

Each read word is sent unconditionally from chassis 3, 4, 9, and 10 to chassis 5 (CP control) and chassis 7 and 8 (CP registers). A read peripheral tag from the stunt box is sent to chassis 4 and then on to chassis 3, 9, and 10. The tag gates the read word to the C^5 register in the read pyramid on PP chassis 1.

The read peripheral tag also enters a time delay chain and is returned to the PP as a resume signal. The resume sets the C^5 full FF in the PP (after data word is in C^5) to signal the presence of the read word. The same resume also clears the central busy FF to indicate to PP control that the address has been accepted by the stunt box and CM has delivered the word. This allows the PPs to proceed and send another address to the stunt box.

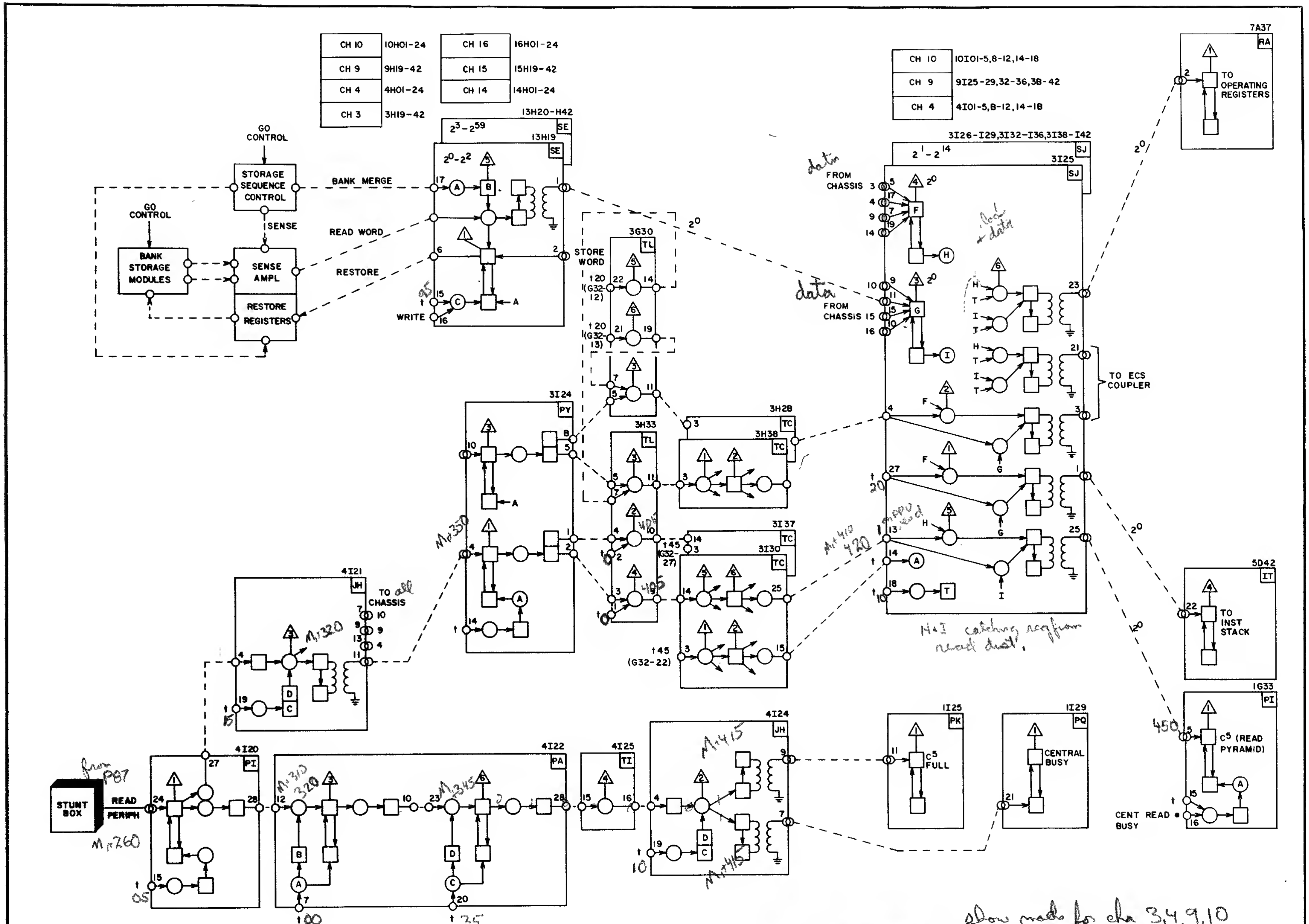


CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE
CENTRAL MEMORY
READ DISTRIBUTOR
SERIALS 1-7

PRODUCT		
6601		
SIZE C	DRAWING NO. 60119300	REV M
SHEET 43	10.1	



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: CENTRAL MEMORY READ DISTRIBUTOR SERIALS 8-UP

PRODUCT: 6601/13
SIZE: C DRAWING NO: 60119300 REV: BT
SHEET: 269 PAGE: 11

from To

Bit	Module	Pin	TP	Module	Pin	TP
59	3H42	28	6	10I18	5	1
58		8	2	17	5	1
57		1	1	16	5	1
56	3H41	28	6	15	5	1
55		8	2	14	5	1
54		1	1	12	5	1
53	3H40	28	6	11	5	1
52		8	2	10	5	1
51		1	1	09	5	1
50	3H89	28	6	08	5	1
49		8	2	05	5	1
48		1	1	04	5	1
47	3H37	28	6	03	5	1
46		8	2	02	5	1
45		1	1	01	5	1
44	3H36	28	6	9I42	5	1
43		8	2	41	5	1
42		1	1	40	5	1
41	3H35	28	6	39	5	1
40		8	2	38	5	1
39		1	1	36	5	1
38	3H34	28	6	35	5	1
37		8	2	34	5	1
36		1	1	33	5	1
35	3H32	28	6	32	5	1
34		8	2	29	5	1
33		1	1	28	5	1
32	3H31	28	6	27	5	1
31		8	2	26	5	1
30		1	1	25	5	1
29	3H30	29	6	4I18	5	1
28		8	2	17	5	1
27		1	1	16	5	1
26	3H29	28	6	15	5	1
25		8	2	14	5	1
24		1	1	12	5	1
23	3H27	28	6	11	5	1
22		8	2	10	5	1
21		1	1	09	5	1
20	3H26	28	6	08	5	1
19		8	2	05	5	1
18		1	1	04	5	1
17	3H25	28	6	03	5	1
16		8	2	02	5	1
15		1	1	01	5	1
14	3H24	28	6	3I42	5	1
13		8	2	41	5	1
12		1	1	40	5	1
11	3H22	28	6	39	5	1
10		8	2	38	5	1
9		1	1	36	5	1
8	3H21	28	6	35	5	1
7		8	2	34	5	1
6		1	1	33	5	1
5	3H20	28	6	32	5	1
4		8	2	29	5	1
3		1	1	28	5	1
2	3H19	28	6	27	5	1
1		8	3	26	5	1
0		1	1	25	5	1
	Read/Dist. Restore →			Read Distributor		

Bit	Module	Pin	TP	Module	Pin	TP
59	4H24	28	6	10I18	3	1
58		8	2	17	3	1
57		1	1	16	3	1
56	4H23	28	6	15	3	1
55		8	2	14	3	1
54		1	1	12	3	1
53	4H22	28	6	11	3	1
52		8	2	10	3	1
51		1	1	09	3	1
50	4H21	28	6	08	3	1
49		8	2	05	3	1
48		1	1	04	3	1
47	4H19	28	6	03	3	1
46		8	2	02	3	1
45		1	1	01	3	1
44	4H18	28	6	9I42	3	1
43		8	2	41	3	1
42		1	1	40	3	1
41	4H17	28	6	39	3	1
40		8	2	38	3	1
39		1	1	36	3	1
38	4H16	28	6	35	3	1
37		8	2	34	3	1
36		1	1	33	3	1
35	4H14	28	6	32	3	1
34		8	2	29	3	1
33		1	1	28	3	1
32	4H13	28	6	27	3	1
31		8	2	26	3	1
30		1	1	25	3	1
29	4H12	28	6	4I18	3	1
28		8	2	17	3	1
27		1	1	16	3	1
26	4H11	28	6	15	3	1
25		8	2	14	3	1
24		1	1	12	3	1
23	4H09	28	6	11	3	1
22		8	2	10	3	1
21		1	1	09	3	1
20	4H08	28	6	08	3	1
19		8	2	05	3	1
18		1	1	04	3	1
17	4H07	28	6	03	3	1
16		8	2	02	3	1
15		1	1	01	3	1
14	4H06	28	6	3I42	3	1
13		8	2	41	3	1
12		1	1	40	3	1
11	4H04	28	6	39	3	1
10		8	2	38	3	1
9		1	1	36	3	1
8	4H03	28	6	35	3	1
7		8	2	34	3	1
6		1	1	33	3	1
5	4H02	28	6	32	3	1
4		8	2	29	3	1
3		1	1	28	3	1
2	4H01	28	6	27	3	1
1		8	2	26	3	1
0		1	1	25	3	1
	Read/Dist. Restore →			Read Distributor		

Bit	Module	Pin	TP	Module	Pin	TP
59	9H42	28	6	10I18	7	1
58		8	2	17	7	1
57		1	1	16	7	1
56	9H41	28	6	15	7	1
55		8	2	14	7	1
54		1	1	12	7	1
53	9H40	28	6	11	7	1
52		8	2	10	7	1
51		1	1	09	7	1
50	9H39	28	6	08	7	1
49		8	2	05	7	1
48		1	1	04	7	1
47	9H37	28	6	03	7	1
46		8	2	02	7	1
45		1	1	01	7	1
44	9H36	28	6	9I42	7	1
43		8	2	41	7	1
42		1	1	40	7	1
41	9H35	28	6	39	7	1
40		8	2	38	7	1
39		1	1	36	7	1
38	9H34	28	6	35	7	1
37		8	2	34	7	1
36		1	1	33	7	1
35	9H32	28	6	32	7	1
34		8	2	29	7	1
33		1	1	28	7	1
32	9H31	28	6	27	7	1
31		8	2	26	7	1
30		1	1	25	7	1
29	9H30	28	6	4I18	7	1
28		8	2	17	7	1
27		1	1	16	7	1
26	9H29	28	6	15	7	1
25		8	2	14	7	1
24		1	1	12	7	1
23	9H27	28	6	11	7	1
22		8	2	10	7	1
21		1	1	09	7	1
20	9H26	28	6	08	7	1
19		8	2	05	7	1
18		1	1	04	7	1
17	9H25	28	6	03	7	1
16		8	2	02	7	1
15		1	1	01	7	1
14	9H24	28	6	3I42	7	1
13		8	2	41	7	1
12		1	1	40	7	1
11	9H22	28	6	39	7	1
10		8	2	38	7	1
9		1	1	36	7	1
8	9H21	28	6	35	7	1
7		8	2	34	7	1
6		1	1	33	7	1
5	9H20	28	6	32	7	1
4		8	2	29	7	1
3		1	1	28	7	1
2	9H19	28	6	27	7	1
1		8	2	26	7	1
0		1	1	25	7	1
	Read/Dist. Restore →			Read Distributor		

Bit	Module	Pin	TP	Module	Pin	TP
59	10H24	28	6	10I18	9	1
58		8	2	17	9	1
57		1	1	16	9	1
56	10H23	28	6	15	9	1
55		8	2	14	9	1
54		1	1	12	9	1
53	10H22	28	6	11	9	1
52		8	2	10	9	1
51		1	1	09	9	1
50	10H21	28	6	08	9	1
49		8	2	05	9	1
48		1	1	04	9	1
47	10H19	28	6	03	9	1
46		8	2	02	9	1
45		1	1	01	9	1
44	10H18	28	6	9I42	9	1
43		8	2	41	9	1
42		1	1	40	9	1
41	10H17	28	6	39	9	1
40		8	2	38	9	1
39		1	1	36	9	1
38	10H16	28	6	35	9	1
37		8	2	34	9	1
36		1	1	33	9	1
35	10H14	28	6	32	9	1
34		8	2	29	9	1
33		1	1	28	9	1
32	10H13	28	6	27	9	1
31		8	2	26	9	1
30		1	1	25	9	1
29	10H12	28	6	4I18	9	1
28		8	2	17	9	1
27		1	1	16	9	1
26	10H11	28	6	15	9	1
25		8	2	14	9	1
24		1	1	12	9	1
23	10H09	28	6	11	9	1
22		8	2	10	9	1
21		1	1	09	9	1
20	10H08	28	6	08	9	1
19		8	2	05	9	1
18		1	1	04	9	1
17	10H07	28	6	03	9	1
16		8	2	02	9	1
15		1	1	01	9	1
14	10H06	28	6	3I42	9	1
13		8	2	41	9	1
12		1	1	40	9	1
11	10H04	28	6	39	9	1
10		8	2	38	9	1
9		1	1	36	9	1
8	10H03	28	6	35	9	1
7		8	2	34	9	1
6		1	1	33	9	1
5	10H02	28	6	32	9	1
4		8	2	29	9	1
3		1	1	28	9	1
2	10H01	28	6	27	9	1
1		8	2	26	9	1
0		1	1	25	9	1
	Read/Dist. Restore →			Read Distributor		

Data Trunks
6601 Central Memory
Read/Distribute/Restore (CH 3, 4, 9, 10)
to Read Distribute (CH 3, 4, 9, 10)
Sheet 1

REV. K 12.0

Bit	Module	Pin	TP	Module	Pin	TP
59	13H42	28	6	10I18	11	1
58		8	2	17	11	1
57		1	1	16	11	1
56	13H41	28	6	15	11	1
55		8	2	14	11	1
54		1	1	12	11	1
53	13H40	28	6	11	11	1
52		8	2	10	11	1
51		1	1	09	11	1
50	13H39	28	6	08	11	1
49		8	2	05	11	1
48		1	1	04	11	1
47	13H37	28	6	03	11	1
46		8	2	02	11	1
45		1	1	01	11	1
44	13H36	28	6	9I42	11	1
43		8	2	41	11	1
42		1	1	40	11	1
41	13H35	28	6	39	11	1
40		8	2	38	11	1
39		1	1	36	11	1
38	14H34	28	6	35	11	1
37		8	2	34	11	1
36		1	1	33	11	1
35	13H32	28	6	32	11	1
34		8	2	29	11	1
33		1	1	28	11	1
32	13H31	28	6	27	11	1
31		8	2	26	11	1
30		1	1	25	11	1
29	13H30	28	6	4I18	11	1
28		8	2	17	11	1
27		1	1	16	11	1
26	13H29	28	6	15	11	1
25		8	2	14	11	1
24		1	1	12	11	1
23	13H27	28	6	11	11	1
22		8	2	10	11	1
21		1	1	09	11	1
20	13H26	28	6	08	11	1
19		8	2	05	11	1
18		1	1	04	11	1
17	13H25	28	6	03	11	1
16		8	2	02	11	1
15		1	1	01	11	1
14	13H24	28	6	3I42	11	1
13		8	2	41	11	1
12		1	1	40	11	1
11	13H22	28	6	39	11	1
10		8	2	38	11	1
9		1	1	36	11	1
8	13H21	28	6	35	11	1
7		8	2	34	11	1
6		1	1	33	11	1
5	13H20	28	6	32	11	1
4		8	2	29	11	1
3		1	1	28	11	1
2	13H19	28	6	27	11	1
1		8	2	26	11	1
0		1	1	25	11	1

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	14H24	28	6	10I18	19	6
58		8	2	17	19	6
57		1	1	16	19	6
56	14H23	28	6	15	19	6
55		8	2	14	19	6
54		1	1	12	19	6
53	14H22	28	6	11	19	6
52		8	2	10	19	6
51		1	1	09	19	6
50	14H21	28	6	08	19	6
49		8	2	05	19	6
48		1	1	04	19	6
47	14H19	28	6	03	19	6
46		8	2	02	19	6
45		1	1	01	19	6
44	14H18	28	6	9H42	19	6
43		8	2	41	19	6
42		1	1	40	19	6
41	14H17	28	6	39	19	6
40		8	2	38	19	6
39		1	1	36	19	6
38	14H16	28	6	35	19	6
37		8	2	34	19	6
36		1	1	33	19	6
35	14H14	28	6	32	19	6
34		8	2	29	19	6
33		1	1	28	19	6
32	14H13	28	6	27	19	6
31		8	2	26	19	6
30		1	1	25	19	6
29	14H12	28	6	4I18	19	6
28		8	2	17	19	6
27		1	1	16	19	6
26	14H11	28	6	15	19	6
25		8	2	14	19	6
24		1	1	12	19	6
23	14H09	28	6	11	19	6
22		8	2	10	19	6
21		1	1	09	19	6
20	14H08	28	6	08	19	6
19		8	2	05	19	6
18		1	1	04	19	6
17	14H07	28	6	03	19	6
16		8	2	02	19	6
15		1	1	01	19	6
14	14H06	28	6	3I42	19	6
13		8	2	41	19	6
12		1	1	40	19	6
11	14H04	28	6	39	19	6
10		8	2	38	19	6
9		1	1	36	19	6
8	14H03	28	6	35	19	6
7		8	2	34	19	6
6		1	1	33	19	6
5	14H02	28	6	32	19	6
4		8	2	29	19	6
3		1	1	28	19	6
2	14H01	28	6	27	19	6
1		8	2	26	19	6
0		1	1	25	19	6

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	15H42	28	6	10I18	21	6
58		8	2	17	21	6
57		1	1	16	21	6
56	15H41	28	6	15	21	6
55		8	2	14	21	6
54		1	1	12	21	6
53	15H40	28	6	11	21	6
52		8	2	10	21	6
51		1	1	09	21	6
50	15H39	28	6	08	21	6
49		8	2	05	21	6
48		1	1	04	21	6
47	14H37	28	6	03	21	6
46		8	2	02	21	6
45		1	1	01	21	6
44	15H36	28	6	9I42	21	6
43		8	2	41	21	6
42		1	1	40	21	6
41	15H35	28	6	39	21	6
40		8	2	38	21	6
39		1	1	36	21	6
38	15H34	28	6	35	21	6
37		8	2	34	21	6
36		1	1	33	21	6
35	15H32	28	6	32	21	6
34		8	2	29	21	6
33		1	1	28	21	6
32	15H31	28	6	27	21	6
31		8	2	26	21	6
30		1	1	25	21	6
29	15H30	28	6	4I18	21	6
28		8	2	17	21	6
27		1	1	16	21	6
26	15H29	28	6	15	21	6
25		8	2	14	21	6
24		1	1	12	21	6
23	15H27	28	6	11	21	6
22		8	2	10	21	6
21		1	1	09	21	6
20	15H26	28	6	08	21	6
19		8	2	05	21	6
18		1	1	04	21	6
17	15H25	28	6	03	21	6
16		8	2	02	21	6
15		1	1	01	21	6
14	15H24	28	6	3I42	21	6
13		8	2	41	21	6
12		1	1	40	21	6
11	15H22	28	6	39	21	6
10		8	2	38	21	6
9		1	1	36	21	6
8	15H21	28	6	35	21	6
7		8	2	34	21	6
6		1	1	33	21	6
5	15H20	28	6	32	21	6
4		8	2	29	21	6
3		1	1	28	21	6
2	15H19	28	6	27	21	6
1		8	2	26	21	6
0		1	1	25	21	6

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	16H24	28	6	10I18	23	6
58		8	2	17	23	6
57		1	1	16	23	6
56	16H23	28	6	15	23	6
55		8	2	14	23	6
54		1	1	12	23	6
53	16H22	28	6	11	23	6
52		8	2	10	23	6
51		1	1	09	23	6
50	16H21	28	6	08	23	6
49		8	2	05	23	6
48		1	1	04	23	6
47	16H19	28	6	03	23	6
46		8	2	02	23	6
45		1	1	01	23	6
44	16H18	28	6	9I42	23	6
43		8	2	41	23	6
42		1	1	40	23	6
41	16H17	28	6	39	23	6
40		8	2	38	23	6
39		1	1	36	23	6
38	16H16	28	6	35	23	6
37		8	2	34	23	6
36		1	1	33	23	6
35	16H14	28	6	32	23	6
34		8	2	29	23	6
33		1	1	28	23	6
32	16H13	28	6	27	23	6
31		8	2	26	23	6
30		1	1	25	23	6
29	16H12	28	6	4I18	23	6
28		8	2	17	23	6
27		1	1	16	23	6
26	16H11	28	6	15	23	6
25		8	2	14	23	6
24		1	1	12	23	6
23	16H09	28	6	11	23	6
22		8	2	10	23	6
21		1	1	09	23	6
20	16H08	28	6	08	23	6
19		8	2	05	23	6
18		1	1	04	23	6
17	16H07	28	6	03	23	6
16		8	2	02	23	6
15		1	1	01	23	6
14	16H06	28	6	3I42	23	6
13		8	2	41	23	6
12		1	1	40	23	6
11	16H04	28	6	39	23	6
10		8	2	38	23	6
9		1	1	36	23	6
8	16H03	28	6	35	23	6
7		8	2	34	23	6
6		1	1	33	23	6
5	16H02	28	6	32	23	6
4		8	2	29	23	6
3		1	1	28	23	6
2	16H01	28	6	27	23	6
1		8	2	26	23	6
0		1	1	25	23	6

Read/Dist. Restore → Read Distributor

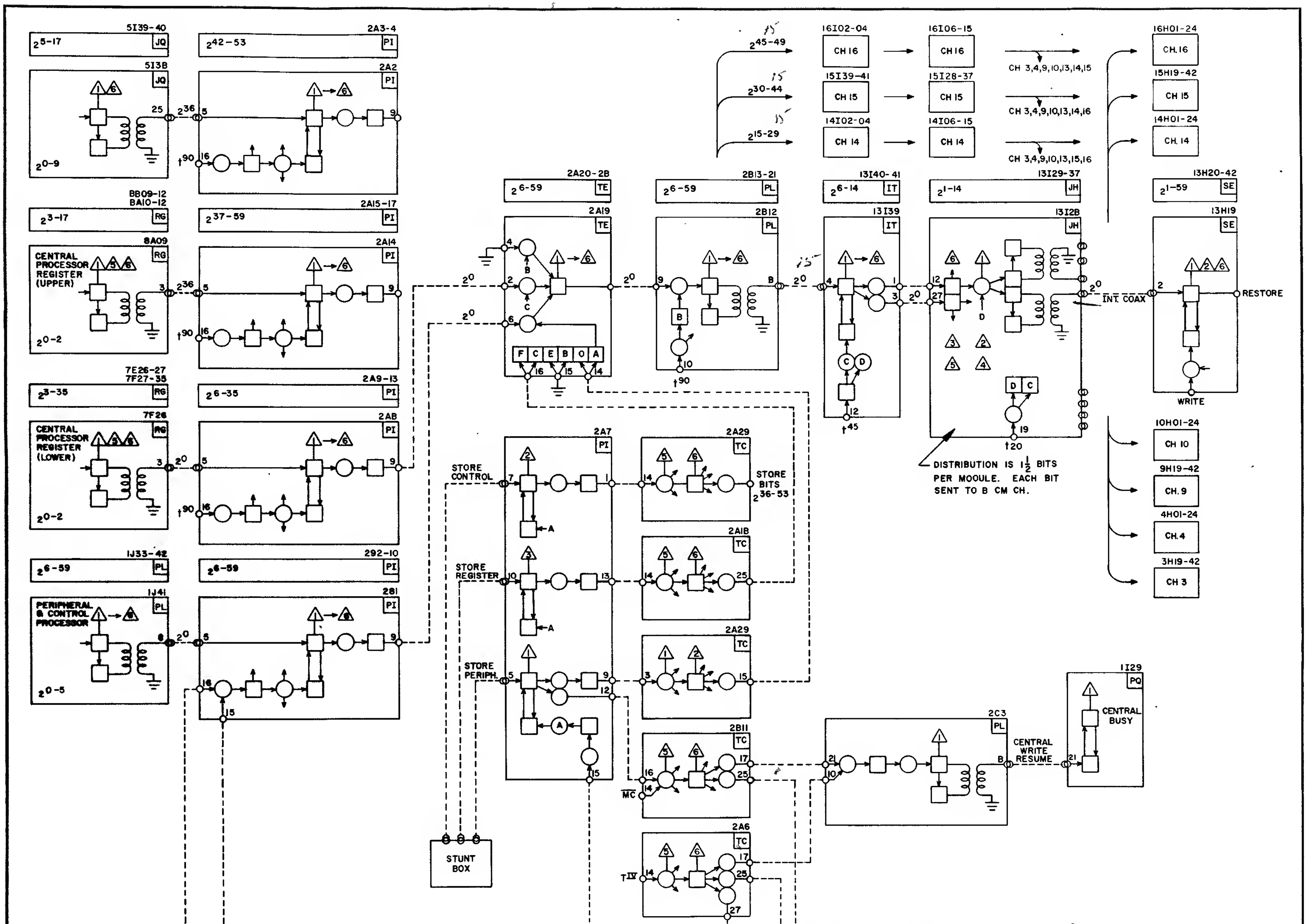
Data Trunks
6601 Central Memory
Read/Distribute/Restore (CH 13, 14, 15, 16)
to Read Distributor (CH 3, 4, 9, 10)
Sheet 2

WRITE DISTRIBUTOR

The write distributor accepts words from the several sources and stores them in 1 of 8 memory chassis. The distributor is on chassis 2. The 60-bit word on chassis 2 is split into four 15-bit groups which are sent to chassis 13-16 respectively. Each of these chassis in turn sends (or stores) its 15-bit group to the other 7 chassis unconditionally.

A 3-to-1 fan-in on chassis 2 selects the proper word under control of the store tag from the stunt box which is established ahead of the data. The word is then split and transmitted to chassis 13-16. The chassis 2 data registers and the tag FFs are cleared simultaneously.

One minor cycle after the register clear, a central write resume is sent to the PP to clear the central busy FF and allow the PPs to send another address to the stunt box.



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE
CENTRAL MEMORY WRITE DISTRIBUTOR SERIALS 1-7

PRODUCT 6601

SIZE C | DRAWING NO. 60119300 | REV K

SHEET 44 | 13

Data Trunks
6601 Central Memory

Store Distributor (CH 2)
to Write Distributor
(CH. 13, 14, 15, 16)

Read Distributor
to Store - Distribute - Restore
(CH. 3, 4, 9, 10)

Sheet 1

Write Dist → Store Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	2B21	23	6	16I04	7	3
58		25	5		6	2
57		27	4		4	1
56		4	3	16I03	22	4
55		6	2		25	5
54		8	1		27	6
53	2B20	23	6		7	3
52		25	5		6	2
51		27	4		4	1
50		4	3	16I02	22	4
49		6	2		25	5
48		8	1		27	6
47	2B19	23	6		7	3
46		25	5		6	2
45		27	4		4	1
44		4	3	15I41	7	3
43		6	2		6	2
42		8	1		4	1
41	2B18	23	6	15I40	22	4
40		25	5		25	5
39		27	4		27	6
38		4	3		7	3
37		6	2		6	2
36		8	1		4	1
35	2B17	23	6	15I39	22	4
34		25	5		25	5
33		27	4		27	6
32		4	3		7	3
31		6	2		6	2
30		8	1		4	1
29	2B16	23	6	14I04	7	3
28		25	5		6	2
27		27	4		4	1
26		4	3	14I03	22	4
25		6	2		25	5
24		8	1		27	6
23	2B15	23	6		7	3
22		25	5		6	2
21		27	4		4	1
20		4	3	14I02	22	4
19		6	2		25	5
18		8	1		27	6
17	2B14	23	6		7	3
16		25	5		6	2
15		27	4		4	1
14		4	3	13I41	7	3
13		6	2		6	2
12		8	1		4	1
11	2B13	23	6	13I40	22	4
10		25	5		25	5
9		27	4		27	6
8		4	3		7	3
7		6	2		6	2
6		8	1		4	1
5	2B12	23	6	13I39	22	4
4		25	5		25	5
3		27	4		27	6
2		4	3		7	3
1		6	2		6	2
0		8	1		4	1

Store Dist → Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	28	6	3H42	24	6
58	16I14	7	2		19	2
57		24	5		2	1
56	16I13	28	6	3H41	24	6
55	16I12	7	2		19	2
54		24	5		2	1
53	16I11	28	6	3H40	24	6
52	16I10	7	2		19	2
51		24	5		2	1
50	16I09	28	6	3H39	24	6
49	16I08	7	2		19	2
48		24	5		2	1
47	16I07	28	6	3H37	24	6
46	16I06	7	2		19	2
45		24	5		2	1
44	15I37	28	6	3H36	24	6
43	15I36	7	2		19	2
42		24	5		2	1
41	15I35	28	6	3H35	24	6
40	15I34	7	2		19	2
39		24	5		2	1
38	15I33	28	6	3H34	24	6
37	15I32	7	2		19	2
36		24	5		2	1
35	15I31	28	6	3H32	24	6
34	15I30	7	2		19	2
33		24	5		2	1
32	15I29	28	6	3H31	24	6
31	15I28	7	2		19	2
30		24	5		2	1
29	14I15	28	6	3H30	24	6
28	14I14	7	2		19	2
27		24	5		2	1
26	14I13	28	6	3H29	24	6
25	14I12	7	2		19	2
24		24	5		2	1
23	14I11	28	6	3H27	24	6
22	14I10	7	2		19	2
21		24	5		2	1
20	14I09	28	6	3H26	24	6
19	14I08	7	2		19	2
18		24	5		2	1
17	14I07	28	6	3H25	24	6
16	14I06	7	2		19	2
15		24	5		2	1
14	13I37	3	1	3H24	24	6
13	13I36	13	3		19	2
12		18	4		2	1
11	13I35	3	1	3H22	24	6
10	13I34	13	3		19	2
9		18	4		2	1
8	13I33	3	1	3H21	24	6
7	13I32	13	3		19	2
6		18	4		2	1
5	13I31	3	1	3H20	24	6
4	13I30	13	3		19	2
3		18	4		2	1
2	13I29	3	1	3H19	24	6
1	13I28	13	3		19	2
0		18	4		2	1

Store Dist → Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I14	5	1	4H24	24	6
58	16I14	11	3		12	2
57		20	4		2	1
56	16I13	5	1	4H23	24	6
55	16I12	11	3		19	2
54		20	4		2	1
53	16I11	5	1	4H22	24	6
52	16I10	11	3		19	2
51		20	4		2	1
50	16I09	5	1	4H21	24	6
49	16I08	11	3		19	2
48		20	4		2	1
47	16I07	5	1	4H19	24	6
46	16I06	11	3		19	2
45		20	4		2	1
44	15I37	5	1	4H18	24	6
43	15I36	11	3		19	2
42		20	4		2	1
41	15I35	5	1	4H17	24	6
40	15I34	11	3		19	2
39		20	4		2	1
38	15I33	5	1	4H16	24	6
37	15I32	11	3		19	2
36		20	4		2	1
35	15I31	5	1	4H14	24	6
34	15I30	11	3		19	2
33		20	4		2	1
32	15I29	5	1	4H13	24	6
31	15I28	11	3		19	2
30		20	4		2	1
29	14I15	5	1	4H12	24	6
28	14I14	11	3		19	2
27		20	4		2	1
26	14I13	5	1	4H11	24	6
25	14I12	11	3		19	2
24		20	4		2	1
23	14I11	5	1	4H09	24	6
22	14I10	11	3		19	2
21		20	4		2	1
20	14I09	5	1	4H08	24	6
19	14I08	11	3		19	2
18		20	4		2	1
17	14I07	5	1	4H07	24	6
16	14I06	11	3		19	2
15		20	4		2	1
14	13I37	5	1	4H06	24	6
13	13I36	11	3		19	2
12		20	4		2	1
11	13I35	5	1	4H04	24	6
10	13I34	11	3		19	2
9		20	4		2	1
8	13I33	5	1	4H03	24	6
7	13I32	11	3		19	2
6		20	4		2	1
5	13I31	5	1	4H02	24	6
4	13I30	11	3		19	2
3		20	4		2	1
2	13I29	5	1	4H01	24	6
1	13I28	11	3		19	2
0		20	4		2	1

Store Dist. → Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	13	3	9H42	24	6
58		18	4		19	2
57	16I14	3	1		2	1
56	16I13	13	3	9H41	24	6
55		18	4		19	2
54	16I12	3	1		2	1
53	16I11	13	3	9H40	24	6
52		18	4		19	2
51	16I10	3	1		2	1
50	16I09	13	3	9H39	24	6
49		18	4		19	2
48	16I08	3	1		2	1
47	16I07	13	3	9H37	24	6
46		18	4		19	2
45	16I06	3	1		2	1
44	15I37	13	3	9H36	24	6
43		18	4		19	2
42	15I36	3	1		2	1
41	15I35	13	3	9H35	24	6
40		18	4		19	2
39	15I34	3	1		2	1
38	15I33	13	3	9H34	24	6
37		18	4		19	2
36	15I32	3	1		2	1
35	15I31	13	3	9H32	24	6
34		18	4		19	2
33	15I30	3	1		2	1
32	15I29	13	3	9H31	24	6
31		18	4		19	2
30	15I28	3	1		2	1
29	14I15	13	3	9H30	24	6
28		18	4		19	2
27	14I14	3	1		2	1
26	14I13	13	3	9H39	24	6
25		18	4		19	2
24	14I12	3	1		2	1
23	14I11	13	3	9H27	24	6
22		18	4		19	2
21	14I10	3	1		2	1
20	14I09	13	3	9H26	24	6
19		18	4		19	2
18	14I08	3	1		2	1
17	14I07	13	3	9H25	24	6
16		18	4		19	2
15	14I06	3	1		2	1
14	13I37	28	6	9H24	24	6
13	13I36	7	2		19	2
12		24	5		2	1
11	13I35	28	6	9H22	24	6
10	13I34	7	2		19	2
9		24	5		2	1
8	13I33	28	6	9H21	24	6
7	13I32	7	2		19	2
6		24	5		2	1
5	13I31	28	6	9H20	24	6
4	13I30	7	2		19	2
3		24	5		2	1
2	13I29	28	6	9H19	24	6
1	13I28	7	2		19	2
0		24	5		2	1

Store Dist → Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	11	3	10H24	24	6
58		20	4		19	2
57	16I14	5	1		2	1
56	16I13	11	3	10H23	24	6
55		20	4		19	2
54	16I12	5	1		2	1
53	16I11	11	3	10H22	24	6
52		20	4		19	2
51	16I10	5	1		2	1
50	16I09	11	3	10H21	24	6
49		20	4		19	2
48	16I08	5	1		2	1
47	16I07	11	3	10H19	24	6
46		20	4		19	2
45	16I06	5	1		2	1
44	15I37	11	3	10H18	24	6
43		20	4		19	2
42	15I36	5	1		2	1
41	15I35	11	3	10H17	24	6
40		20	4		19	2
39	15I34	5	1		2	1
38	15I33	11	3	10H16	24	6
37		20	4		19	2
36	15I32	5	1		2	1
35	15I31	11	3	10H14	24	6
34		20	4		19	2
33	15I30	5	1		2	1
32	15I29	11	3	10H13	24	6
31		20	4		19	2
30	15I28	5	1		2	1
29	14I15	11	3	10H12	24	6
28		20	4		19	2
27	14I14	5	1		2	1
26	14I13	11	3	10H11	24	6
25		20	4		19	2
24	14I12	5	1		2	1
23	14I11	11	3	10H09	24	6
22		20	4		19	2
21	14I10	5	1		2	1
20	14I09	11	3	10H08	24	6
19		20	4		19	2
18	14I08	5	1		2	1
17	14I07	11	3	10H07	24	6
16		20	4		19	2
15	14I06	5	1		2	1
14	13I37	13	3	10H06	24	6
13		18	4		19	2
12	13I36	3	1		2	1
11	13I35	13	3	10H04	24	6
10		18	4		19	2
9	13I34	3	1		2	1
8	13I33	13	3	10H03	24	6
7		18	4		19	2
6	13I32	3	1		2	1
5	13I31	13	3	10H02	24	6
4		18	4		19	2
3	13I30	3	1		2	1
2	13I29	13	3	10H01	24	6
1		18	4		19	2
0	13I28	3	1		2	1

REV. K 14.0

Bit	Module	Pin	TP	Module	Pin	TP
59	2B21	23	6	16I04	7	3
58		25	5		6	2
57		27	4		4	1
56		4	3	16I03	22	4
55		6	2		25	5
54		8	1		27	6
53	2B20	23	6		7	3
52		25	5		6	2
51		27	4		4	1
50		4	3	16I02	22	4
49		6	2		25	5
48		8	1		27	6
47	2B19	23	6		7	3
46		25	5		6	2
45		24	4		4	1
44		4	3	15I41	7	3
43		6	2		6	2
42		8	1		4	1
41	2B18	23	6	15I40	22	4
40		25	5		25	5
39		27	4		27	6
38		4	3		7	3
37		6	2		6	2
36		8	1		4	1
35	2B17	2	6	15I39	22	4
34		2	5		25	5
33		2	4		27	6
32		4	3		7	3
31		6	2		6	2
30		8	1		4	1
29	2B16	23	6	14I04	7	3
28		25	5		6	2
27		2.	4		4	1
26		4	3	14I03	22	4
25		6	2		25	5
24		8	1		27	6
23	2B15	2	6		7	3
22		2	5		6	2
21		27	4		4	1
20		4	3	14I02	22	4
19		6	2		25	5
18		8	1		27	6
17	2B14	23	6		7	3
16		25	5		6	2
15		27	4		4	1
14		4	3	13I41	7	3
13		6	2		6	2
12		8	1		4	1
11	2B13	23	6	13I40	22	4
10		25	5		25	5
9		27	4		27	6
8		4	3		7	3
7		6	2		6	2
6		8	1		4	1
5	2B12	23	6	13I39	22	4
4		25	5		25	5
3		27	4		27	6
2		4	3		7	3
1		6	2		6	2
0		8	1		4	1

Write Dist — Store Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	3	1	13H42	24	6
58	16I14	13	3		19	2
57		18	4		2	1
56	16I13	3	1	13H41	24	6
55	16I12	13	3		19	2
54		18	4		2	1
53	16I11	3	1	13H40	24	6
52	16I10	13	3		19	2
51		18	4		2	1
50	16I09	3	1	13H39	24	6
49	16I08	13	3		19	2
48		18	4		2	1
47	16I07	3	1	13H37	24	6
46	16I06	13	3		19	2
45		18	4		2	1
44	15I37	3	1	13H36	24	6
43	15I36	13	3		19	2
42		18	4		2	1
41	15I35	3	1	13H35	24	6
40	15I34	13	3		19	2
39		18	4		2	1
38	15I33	3	1	13H34	24	6
37	15I32	13	3		19	2
36		18	4		2	1
35	15I31	3	1	13H32	24	6
34	15I30	13	3		19	2
33		18	4		2	1
32	15I29	3	1	13H31	24	6
31	15I28	13	3		19	2
30		18	4		2	1
29	14I15	3	1	13H30	24	6
28	14I14	13	3		19	2
27		18	4		2	1
26	14I13	3	1	13H29	24	6
25	14I12	13	3		19	2
24		18	4		2	1
23	14I11	3	1	13H27	24	6
22	14I10	13	3		19	2
21		18	4		2	1
20	14I09	3	1	13H26	24	6
19	14I08	13	3		19	2
18		18	4		2	1
17	14I07	3	1	13H25	24	6
16	14I06	13	3		19	2
15		18	4		2	1
14	13I37	26	6	13H24	24	6
13	13I36	9	2		19	2
12		22	5		2	1
11	13I35	26	6	13H22	24	6
10	13I34	9	2		19	2
9		22	5		2	1
8	13I33	26	6	13H21	24	6
7	13I32	9	2		19	2
6		22	5		2	1
5	13I31	26	6	13H20	24	6
4	13I30	9	2		20	2
3		22	5		2	1
2	13I29	26	6	13H19	24	6
1	13I28	9	2		19	2
0		22	5		2	1

Store Dist — Read Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	9	2	14H24	24	6
58		22	5		19	2
57	16I14	26	6		2	1
56	16I13	9	2	14H23	24	6
55		22	5		19	2
54	16I12	26	6		2	1
53	16I11	9	2	14H22	24	6
52		22	5		19	2
51	16I10	26	6		2	1
50	16I09	9	2	14H21	24	6
49		22	5		19	2
48	16I08	26	6		2	1
47	16I07	9	2	14H19	24	6
46		22	5		19	2
45	16I06	26	6		2	1
44	15I37	9	2	14H18	24	6
43		22	5		19	2
42	15I36	26	6		2	1
41	15I35	9	2	14H17	24	6
40		22	5		19	2
39	15I34	26	6		2	1
38	15I33	9	2	14H16	24	6
37		22	5		19	2
36	15I32	26	6		2	1
35	15I31	9	2	14H14	24	6
34		22	5		19	2
33	15I30	26	6		2	1
32	15I29	9	2	14H13	24	6
31		22	5		19	2
30	15I28	26	6		2	1
29	14I15	26	6	14H12	24	6
28	14I14	9	2		19	2
27		22	5		2	1
26	14I13	26	6	14H11	24	6
25	14I12	9	2		19	2
24		22	5		2	1
23	14I11	26	6	14H09	24	6
22	14I10	9	2		19	2
21		22	5		2	1
20	14I09	26	6	14H08	24	6
19	14I08	9	2		19	2
18		22	5		2	1
17	14I07	26	6	14H07	24	6
16	14I06	9	2		19	2
15		22	5		2	1
14	13I37	11	3	14H06	24	6
13		20	4		19	2
12	13I36	5	1		2	1
11	13I35	11	3	14H04	24	6
10		20	4		19	2
9	13I34	5	1		2	1
8	13I33	11	3	14H0	24	6
7		20	4		19	2
6	13I32	5	1		2	1
5	13I31	11	3	14H02	24	6
4		20	4		19	2
3	13I30	5	1		2	1
2	13I29	11	3	14H01	24	6
1		20	4		19	2
0	13I28	5	1		2	1

Store Dist — Read Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	7	2	15H42	24	6
58		24	5		19	2
57	16I14	28	6		2	1
56	16I13	7	2	15H41	24	6
55		24	5		19	2
54	16I12	28	6		2	1
53	16I11	7	2	15H40	24	6
52		24	5		19	2
51	16I10	28	6		2	1
50	16I09	7	2	15H39	24	6
49		24	5		19	2
48	16I08	28	6		2	1
47	16I07	7	2	15H37	24	6
46		24	5		19	2
45	16I06	28	6		2	1
44	15I37	26	6	15H36	24	6
43	15I36	9	2		19	2
42		22	5		2	1
41	15I35	26	6	15H35	24	6
40	15I34	9	2		19	2
39		22	5		2	1
38	15I33	26	6	15H34	24	6
37	15I32	9	2		19	2
36		22	5		2	1
35	15I31	26	6	15H32	24	6
34	15I30	9	2		19	2
33		22	5		2	1
32	15I29	26	6	15H31	24	6
31	15I28	9	2		19	2
30		22	5		2	1
29	14I15	9	2	15H30	24	6
28		22	5		19	2
27	14I14	26	6		2	1
26	14I13	9	2	15H29	24	6
25		22	5		19	2
24	14I12	26	6		2	1
23	14I11	9	2	14H27	24	6
22		22	5		19	2
21	14I10	26	6		2	1
20	14I09	9	2	14H26	24	6
19		22	5		19	2
18	14I08	26	6		2	1
17	14I07	9	2	15H25	24	6
16		22	5		19	2
15	14I06	26	6		2	1
14	13I37	9	2	15H24	24	6
13		22	5		19	2
12	13I36	26	6		2	1
11	13I35	9	2	15H22	24	6
10		22	5		19	2
9	13I34	26	6		2	1
8	13I33	9	2	15H21	24	6
7		22	5		19	2
6	13I32	26	6		2	1
5	13I31	9	2	15H20	24	6
4		22	5		19	2
3	13I30	26	6		2	1
2	13I29	9	2	15H19	24	6
1		22	5		19	2
0	13I28	26	6		2	1

Store Dist — Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I15	26	6	16H24	24	6
58	16I14	9	2		19	2
57		22	5		2	1
56	16I13	26	6	16H23	24	6
55	16I12	9	2		19	2
54		22	5		2	1
53	16I11	26	6	16I11	26	6
52	16I10	9	2		19	2
51		22	5		2	1
50	16I09	26	6	16H21	24	6
49	16I08	9	2		19	2
48		22	5		2	1
47	16I07	26	6	16H19	24	6
46	16I06	9	2		19	2
45		22	5		2	1
44	15I37	7	2	16H18	24	6
43		24	5		19	2
42	15I36	28	6		2	1
41	15I35	7	2	16H17	24	6
40		24	5		19	2
39	15I34	28	6		2	1
38	15I33	7	2	16H16	24	6
37		24	5		19	2
36	15I32	28	6		2	1
35	15I31	7	2	16H14	24	6
34		24	5		19	2
33	15I30	28	6		2	1
32	15I29	7	2	16H13	24	6
31		24	5		19	2
30	15I28	28	6		2	1
29	14I15	7	2	16H12	24	6
28		24	5		19	2
27	14I14	28	6		2	1
26	14I13	7	2	16H11	24	6
25		24	5		19	2
24	14I12	28	6		2	1
23	14I11	7	2	16H09	24	6
22		24	5		19	2
21	14I10	28	6		2	1
20	14I09	7	2	16H08	24	6
19		24	5		19	2
18	14I08	28	6		2	1
17	14I07	7		16H07	24	6
16		24	5		19	2
15	14I06	28	6		2	1
14	13I37	7	2	16H06	24	6
13		24	5		19	2
12	13I36	28	6		2	1
11	13I35	7	2	16H04	24	6
10		24	5		19	2
9	13I34	28	6		2	1
8	13I33	7	2	16H03	24	6
7		24	5		19	2
6	13I32	28	6		2	1
5	13I31	7	2	16H02	24	6
4		24	5		19	2
3	13I30	28	6		2	1
2	13I29	7	2	16H0,1	24	6
1		24	5		19	2
0	18I28	28	6		2	1

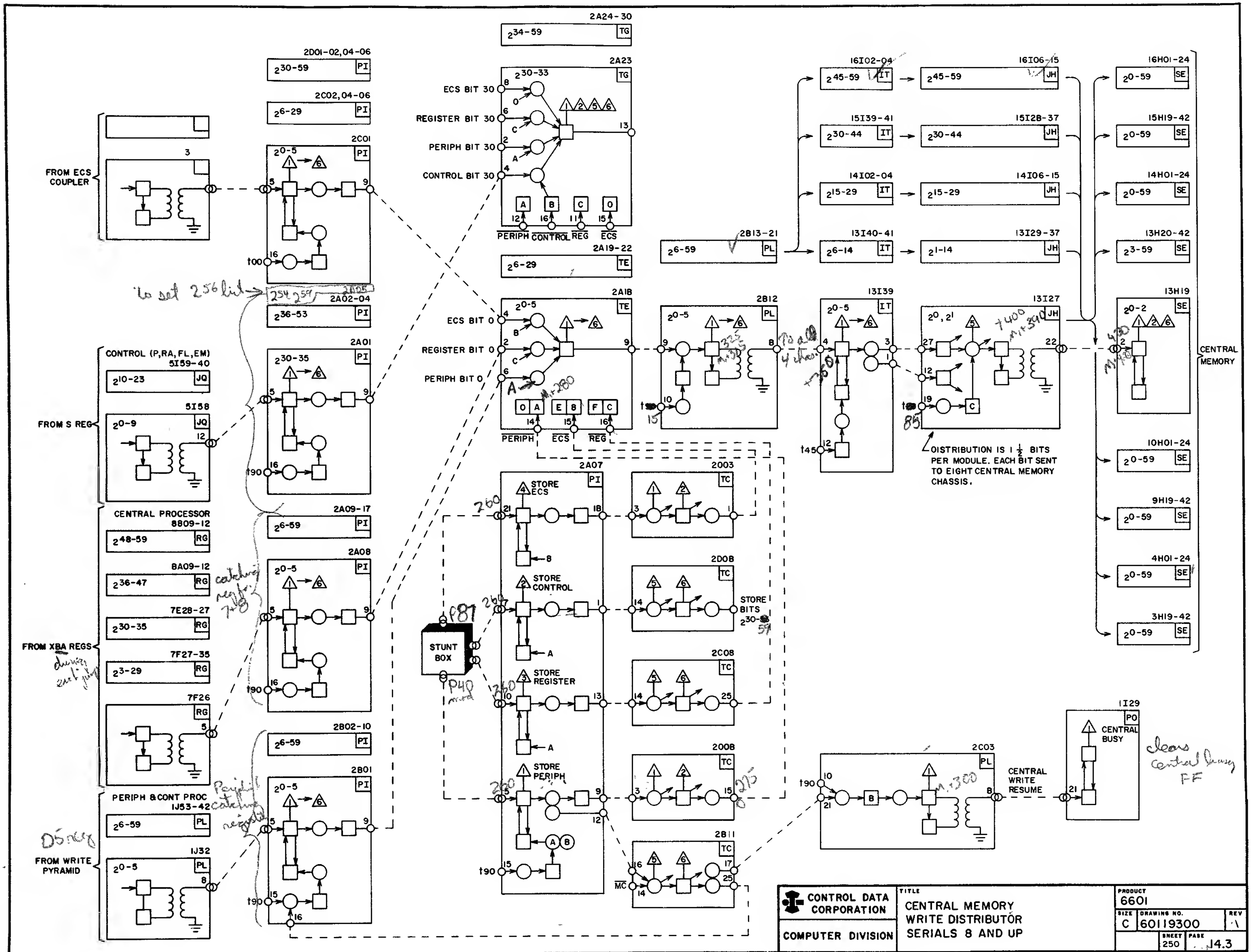
Store Dist — Read/ Dist/ Restore

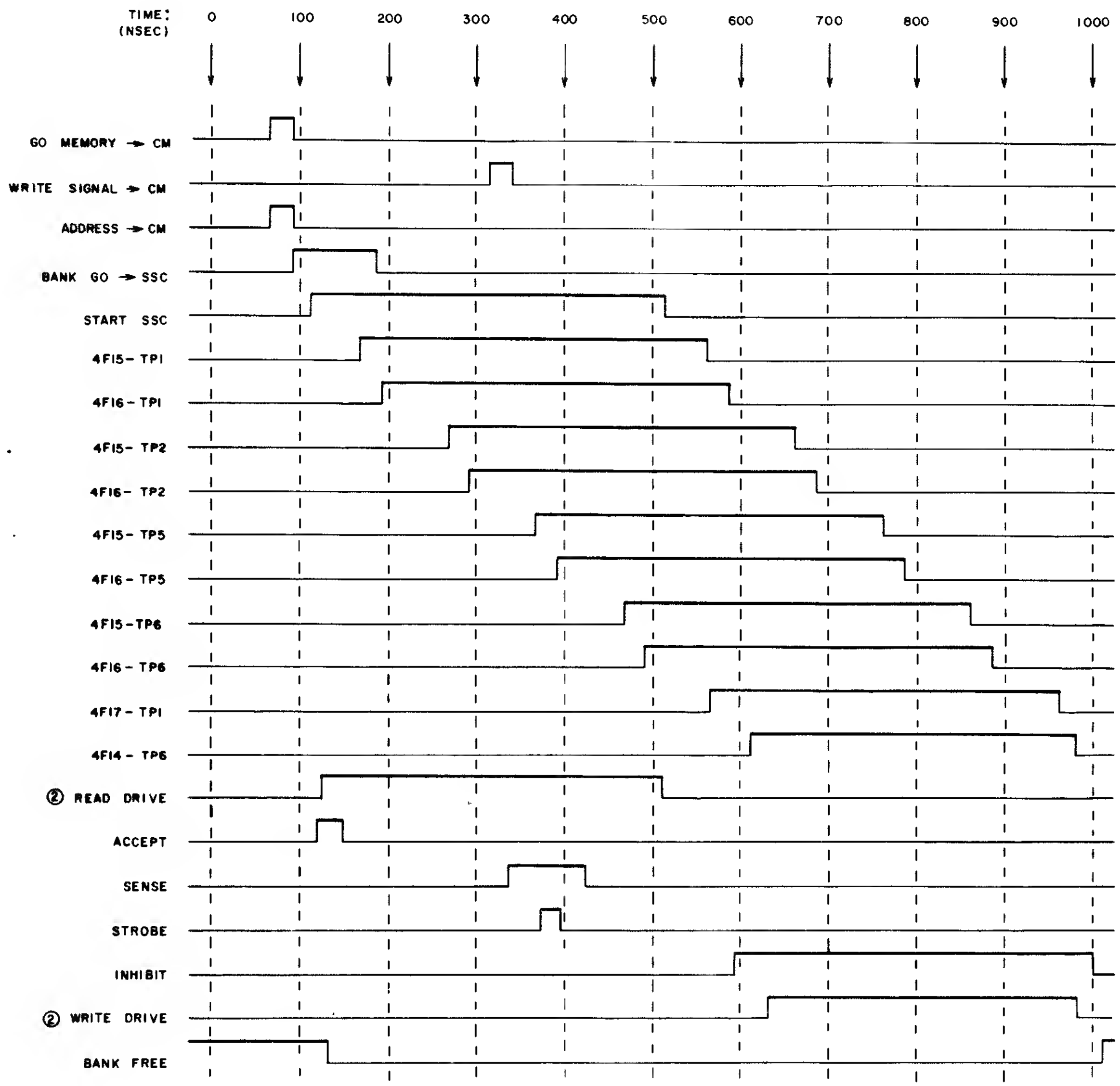
Data Trunks
6601 Central Memory

Store Distributor (CH 2)
to Write Distributor (CH 13, 14, 15, 16)

Store Distributor
to Read-Distribute-Restore
(CH 13, 14, 15, 16)

Sheet 2


FROM ECS COUPLER
FROM S REG
CONTROL (P,RA,FL,EM) 5I59-40
2^{10-23} JQ
5I58
2^{0-9} JQ
CENTRAL PROCESSOR 8809-12
2^{48-59} RG
8A09-12
2^{36-47} RG
7E28-27
2^{30-35} RG
7F27-35
2^{3-29} RG
7F26
FROM XBA REGS
PERIPH & CONT PROC 1J53-42
2^{6-59} PL
1J32
2^{0-5} PL
FROM WRITE PYRAMID
2D01-02,04-06
2^{30-59} PI
2C02,04-06
2^{6-29} PI
2C01
2A02-04
2^{36-53} PI
2A01
2^{30-35} PI
2A09-17
2^{6-59} PI
2A08
2B02-10
2^{6-59} PI
2B01
2A24-30
2^{34-59} TG
2A23
ECS BIT 30
REGISTER BIT 30
PERIPH BIT 30
CONTROL BIT 30
PERIPH CONTROL REG ECS
2A19-22
2^{6-29} TE
2A18
ECS BIT 0
REGISTER BIT 0
PERIPH BIT 0
PERIPH ECS REG
2A07
STORE ECS
STORE CONTROL
STORE REGISTER
STORE PERIPH
STUNT BOX
2D03
2D08
STORE BITS 2^{30-59}
2C08
2D08
2B11
2B13-21
2^{6-59} PL
2B12
16I02-04
2^{45-59} IT
15I39-41
2^{30-44} IT
14I02-04
2^{15-29} IT
13I40-41
2^{6-14} IT
13I39
16I06-15
2^{45-59} JH
15I28-37
2^{30-44} JH
14I06-15
2^{15-29} JH
13I29-37
2^{1-14} JH
13I27
DISTRIBUTION IS $1\frac{1}{2}$ BITS PER MODULE. EACH BIT SENT TO EIGHT CENTRAL MEMORY CHASSIS.
16H01-24
2^{0-59} SE
15H19-42
14H01-24
13H20-42
2^{3-59} SE
13H19
10H01-24
9H19-42
4H01-24
3H19-42
CENTRAL MEMORY
2C03
CENTRAL WRITE RESUME
1I29
CENTRAL BUSY
to set 256 bit
catching regs for 7-8
during exit jump
Periph catching register
D5 reg
clears central busy FF
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY WRITE DISTRIBUTOR SERIALS 8 AND UP
PRODUCT 6601
SIZE C
DRAWING NO. 60119300
SHEET 250
PAGE 14.3



NOTES:

1. STORAGE CYCLE TIMING IS TYPICAL FOR ALL MEMORY CHASSIS (CHASSIS 4, BANK 00 LOCATIONS AND TP'S SHOWN).

② READ/WRITE DRIVE TIMES SHOWN ARE THAT OF OUTPUT PINS ON 4F14

THIS SHEET IS IDENTICAL TO CENTRAL MEMORY (131K) PAGE 15

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY STORAGE CYCLE TIMING	PRODUCT 6601/04		
		SIZE C	DRAWING NO 60119300	REV BT
		SHEET 45	PAGE 15	

CENTRAL MEMORY (65K)
CONTENTS

Pub. No. 60119300
Rev. M

ADDRESSING

The CP programs are stored in CM, and all PPs may use CM for supplementary storage or inter-communication control. Thus CM addresses are generated by the CP and all PPs.

Each processor sends a CM address to a common address clearing house, or stunt box, from where they are sent on to CM. The stunt box can accept addresses from the several sources at 100-nsec intervals (maximum rate) on a priority basis and in turn issue one address every 100 nsec to CM.

An address goes to all banks of CM for decoding, and the referenced bank returns an accept signal to the stunt box if the bank is not busy (free) with a previous reference. The stunt box saves each address that it sends to CM in a hopper mechanism, and, if the address is not accepted, it si recovered from the hopper and re-issued to CM and again saved. The issue-save cycle repeats until an accept is received to void the hopper address. Up to three addresses can be saved in the hopper. However, an address is always accepted within 2000 nsec (worst case because of bank conflict) of the first time it is issued.

DATA DISTRIBUTION

Data to and from CM is distributed from a data distributor. The word from a read reference goes from CM to the data distributor and then to the requesting processor. A word to be stored during a write reference goes from the processor to the data distributor to CM. The distributor can transfer a word to or from CM every 100 nsec. A store word goes to all banks of CM, but separate storage control mechanisms for each bank insure that the word is stored in the proper bank.

The distributor routes data to and from proper origins and destinations as directed by control information or tags received from the stunt box. The tags are entered in the stunt box along with each address and serve to identify the address sender, origin or destination of data, and nature of the address, e.g., read, write, or PP exchange jump. The stunt box sends the tags to the data distributor (and to destinations in the processors for read references) when an address is accepted, and the distributor accomplishes the data transmission. For write references, the data source sends the word to the distributor, where it is held temporarily before it is stored.

STORAGE

The many banks of storage in CM are evenly distributed on 4 chassis in the computer. There are four banks per chassis.

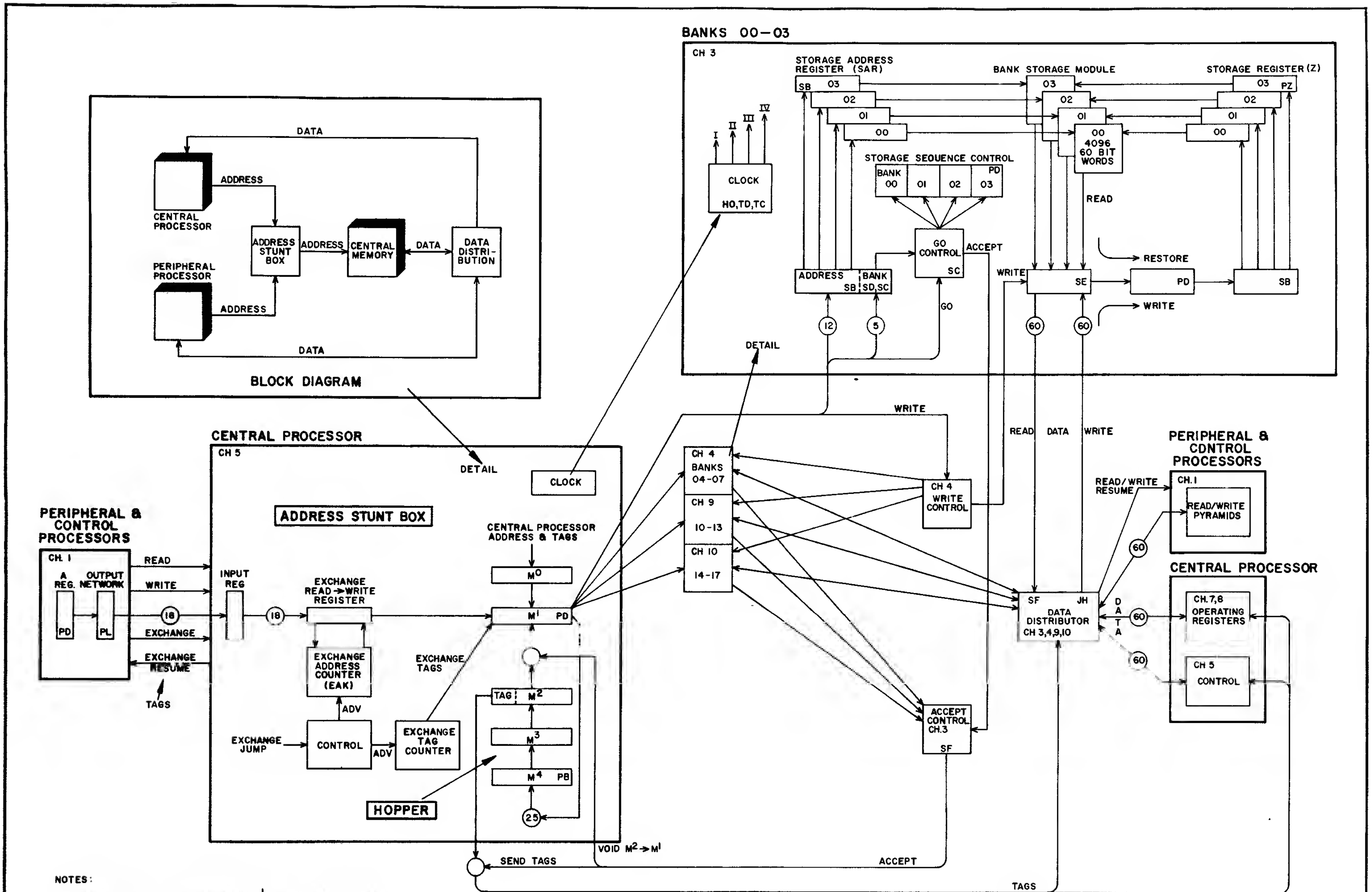
The circuit organization allows the four banks to operate independently and be phased into operation at 100-nsec intervals, which corresponds to the maximum rate at which the stunt box issues addresses. A chassis input register receives the 17-bit address from the stunt box and distributes the 12-bit address to 1 of 4 storage address registers associated with the four banks. Hence 16 consecutive addresses referencing 16 separate banks may be accepted at 16 consecutive minor cycle intervals and result in a data word flowing to or from CM in 16 consecutive minor cycle intervals. The independent controls for each bank and treatment of the address and data word insure that only one bank is in a given time segment of its 1000 nsec storage cycle at any one time. At least one minor cycle separates the storage cycle of all banks.

A word read from any bank is sent to a common temporary storage register and to the data distributor by a common path. A word to be restored is then sent to a write register by way of a buffer register.. The write register sends the word to 1 or 4 restoration registers for restoring in the proper bank.

A word from the data distributor during a write reference goes to the temporary storage register on all chassis and then follows the restore path for writing in memory. Only one of the many banks is in the proper time spot in its storage cycle to store the word recieved, and this bank is the one associated with the write address.

A go signal with each address from the stunt box allows a group of four banks (one chassis) to recognize and translate the bank bits. The referenced bank, if not busy, sends an accept to the stunt box and starts 1 of 4 storage sequence control circuits, which in turn direct the 1000 nsec storage cycle for the selected address.

A write signal may also accompany each address from the stunt box. It distinguishes read and write references and controls the path to the restoration registers. The CM uses the same 12-bit storage module as used in the PPs, but five are driven in parallel to hold the 60-bit word.



NOTES:

1. ADDRESSES SENT TO CM FROM M^1 AT MINOR CYCLE RATE.
2. DATA MOVES TO/FROM CM AT MINOR CYCLE RATE.
3. ADDRESS TAGS DEFINE ORIGIN / DESTINATION OF DATA.
4. TIME FROM $M^1 \rightarrow$ CM TO RESPONSE TO CM ACCEPT IS 200 NSEC.
   a. M^1 STORED IN M^4 AT ISSUE TIME AND MOVES TO M^2 IN TIME SEQUENCE.
   b. ACCEPT VOIDS RE-ISSUE OF ADDRESS FROM HOPPER.

CONTROL DATA CORPORATION	TITLE	PRODUCT 6604	
COMPUTER DIVISION	CENTRAL MEMORY (65K) ADDRESS - DATA FLOW	SIZE C, DRAWING NO. 60119300	REV K
		SHEET 242	1

GO CONTROL (65K)

A go control circuit is associated with each chassis (four banks) of CM. The circuit has several functions.

1. Recognize an address from the stunt box and determine if it is located in an associated bank.
2. Sends an accept to the stunt box if the address is valid and the bank if free.
3. Starts the 1000 nsec storage cycle to read or store the word at the selected address.

No accept is sent to the stunt box if the selected bank is executing a storage cycle from a previously issued address (bank busy case). The address is ignored in this case. The time of address issue from the stunt box and the time the accept should be recieved back at the stunt box is 200 nsec, and this time is used by the stunt box to determine if the address has been accepted. An accept at the proper time voids reissue of the address; otherwise address reissue continues until the accept is received.

BANK SELECTION

The go signal accompanying each address signals all CM go control circuits to search the bank selection bits and determine if the 12-bit address is located in one of its associated banks. A translator circuit in each go control translates the lower five bits of the address, stores the selection in a FF (one FF for each bank), sends the accept, and starts the storage sequence control circuit to start the storage cycle.

The five bits provide 16 unique codes, one for each bank. The upper three bits select 1 of 4 chassis and the lower two bits 1 of 4 banks on the chassis.

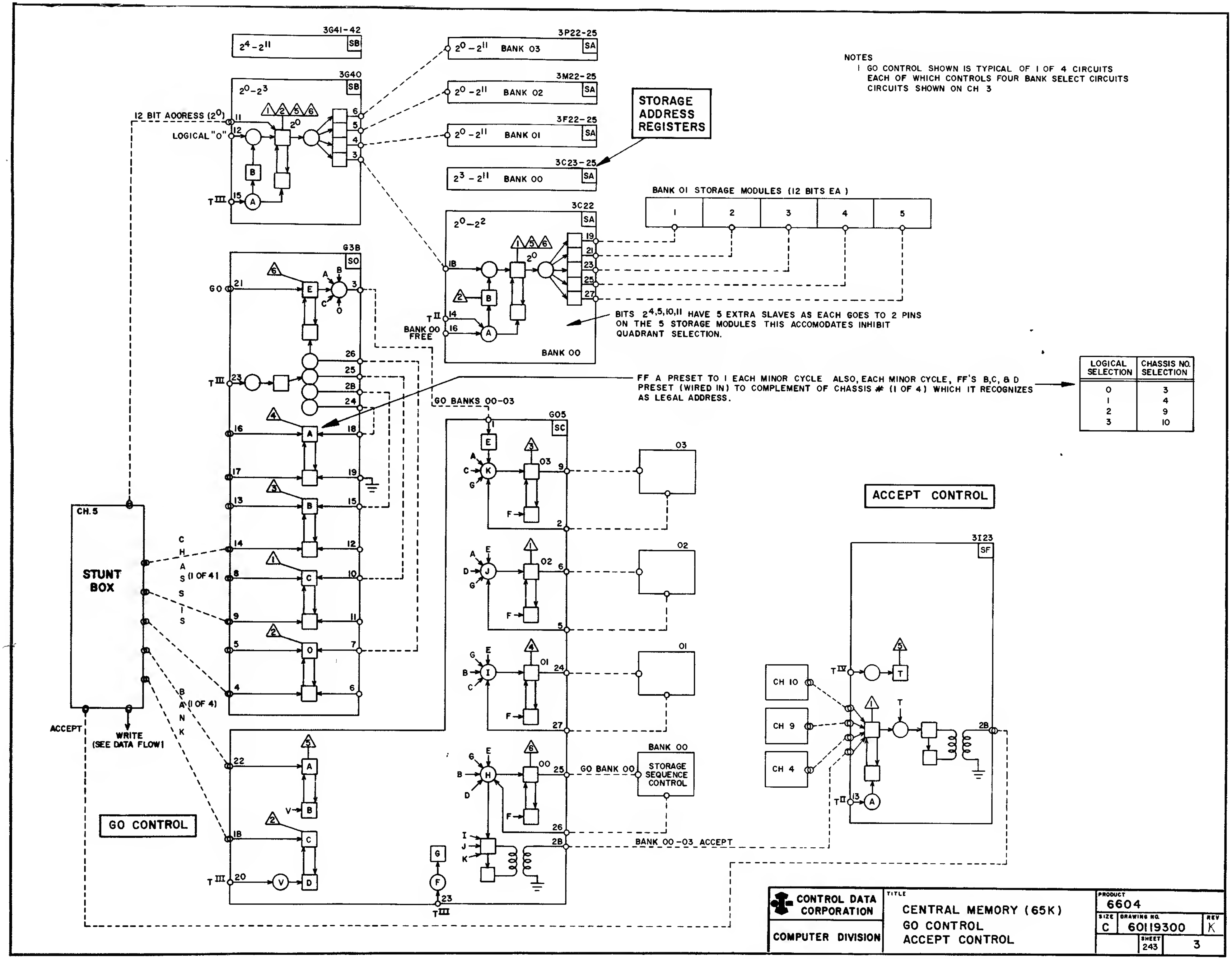
The 17-bit address and bank quantity is stored in an input FF register. Before an address is received, a clock pulse presets the upper three of the five bank bits to the complement of the quantity it should recognize. Thus, for a zero chassis selection (physical chassis 3), the upper three bits are preset to 111XX, the complement of 000XX. A 000XX bank code then is necessary to complete the go FF output gate, which in turn allows recognition of the lower two bits of the bank selection.

Four unique translations are made from the lower two bits of the bank selection bits and stored in separate FFs. A go from the 1 of 8 translator, a bank free condition from the storage sequence control circuit, and a clock pulse gates the 1 of 4 storage and turns on the accept signal. The set FF then starts an associated storage sequence control circuit.

ACCEPT CONTROL

The accept signal indicates a bank is free and has accepted the address in its chassis input register. The time interval from address issue from the stunt box to receipt of the accept in the stunt box allows the stunt box to determine if the address has been accepted. If so, the address in the stunt box hopper is destroyed, and address tags are sent from the stunt box to the data distributor and other areas to tell the address sender to send its data word (write reference) or be ready for receipt of the word read (read reference).

One accept is associated with each chassis for a maximum of eight signals. All are combined in a common OR circuit which feeds the stunt box. Since an address may be sent each 100 nsecs, an accept may be sent to the stunt box every 100 nsecs, with each accept delayed from its associated address by 200 nsecs.



LOGICAL SELECTION	CHASSIS NO. SELECTION
0	3
1	4
2	9
3	10

NOTES
1 GO CONTROL SHOWN IS TYPICAL OF 1 OF 4 CIRCUITS EACH OF WHICH CONTROLS FOUR BANK SELECT CIRCUITS CIRCUITS SHOWN ON CH 3

CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
CENTRAL MEMORY (65K)
GO CONTROL
ACCEPT CONTROL

PRODUCT	SIZE	DRAWING NO.	REV	SHEET	
6604	C	60119300	K	243	3

STORAGE SEQUENCE CONTROL

Storage sequence control responds to a bank go condition from go control and generates a series of timing signals which direct the basic cycle of the storage module. In general, the circuit establishes the bank free condition, makes the address available to the storage module, and then issues read, sense, start and end inhibit, bank merge, and write drive signals to sequence reading and writing. The sense signal samples the differential amplifier which receives the data word read out on the double-ended sense lines from storage. The signals time the basic pulse sequence of the 1000 nsec storage cycle. The storage module discussion details the circuits which respond to the address and read and write drive signals, and thereby make the read word available on the sense lines, or store the word to be written or restored in memory.

TIMING CHAIN

The timing chain is a series chain of FFs whose outputs drive slave inverters, which in turn supply the various signals to sequence reading and writing in CM. A pulse enters the chain and is transferred to successive FFs at 50 nsec intervals. A bank go signal sets the read FF to start the sequence. Each FF is set for 400 nsecs; slave inverters from set and cleared FFs in the chain are combined to establish timed gating signals for the various drive signals.

BANK FREE

The bank free condition is established when all FFs in the chain are cleared, i. e., no pulse is travelling down the chain. The read FF, an intermediate FF, and write FFs (last FF in chain), contribute timing signals to the bank free circuit and indicate whether a pulse is in the chain. All three FFs must be cleared to signal bank free, but their set states overlap to signal bank busy when a pulse is in the chain.

The bank free signal allows go control to respond to its back translation circuits and issue a bank go signal which sets the read FF to turn off the bank free signal.

STORAGE CYCLE TIMING

The following are the recommended times or timing durations for Central Memory in all 6000 series computers:

Strobe (time 75 $\pm$ 5 nsec)

This is measured on TP5 of the SE module, (see page 8. 1). This time should be adjusted by varying the length of wire to pin 16 of the SG module.

Read-On (255 nsec $\pm$ 5 nsec) before Strobe.

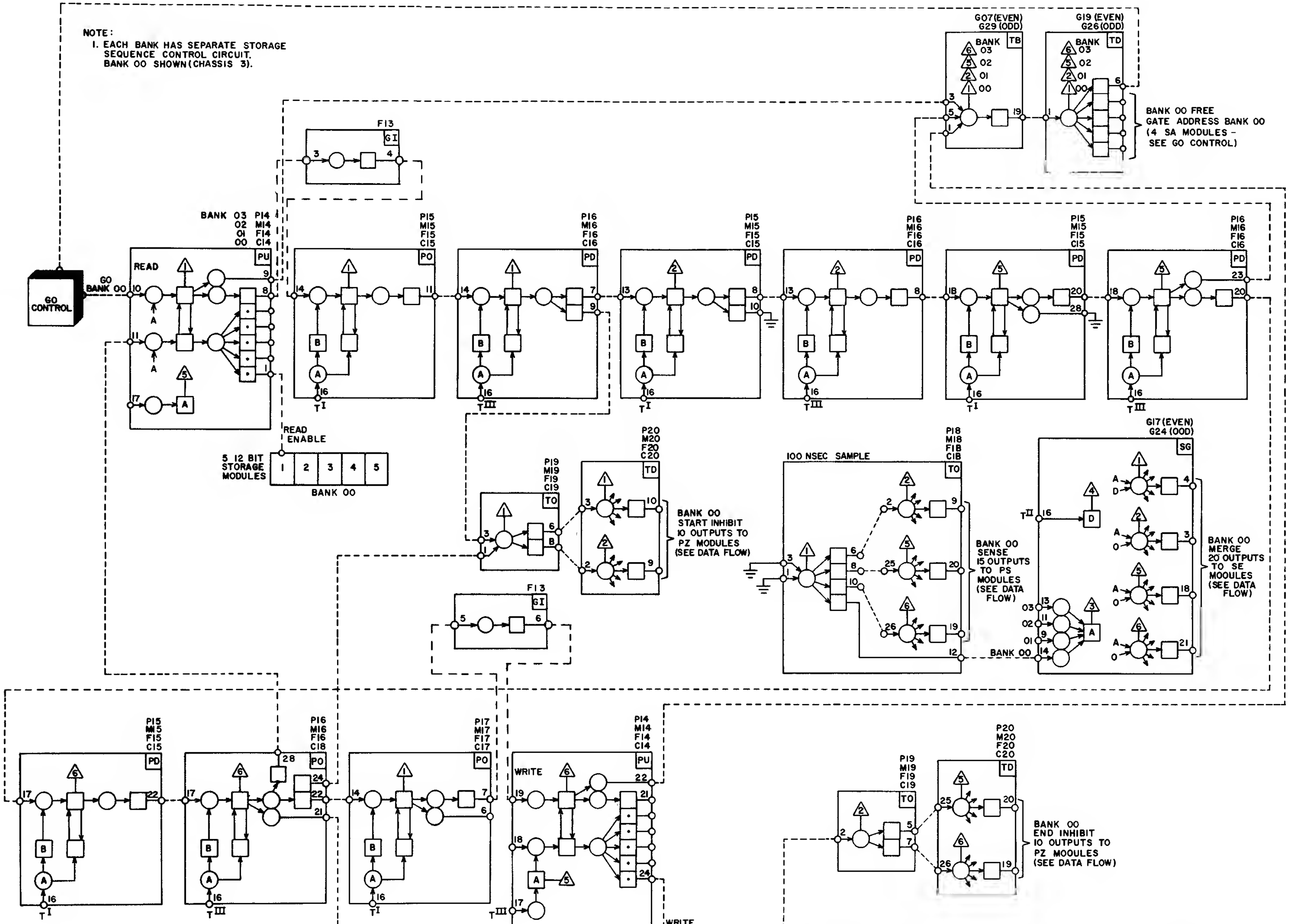
This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 10 of the PU module and/or pin 2 of the GI module.

Read-Off(395 nsec $\pm$ 5 nsec)after the start of Read.

This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 11 of the PU module.

Write (355 nsec $\pm$ 5 nsec)

This is measured on pin 24 of the PU module. This time should be adjusted by varying the length of wire to pin 19 of the PU module and/or pin 5 of the GI module. See also page 8. 1.



CONTROL DATA CORPORATION	TITLE: CENTRAL MEMORY (65K) STORAGE SEQUENCE CONTROL	PRODUCT: 6604	
COMPUTER DIVISION		SIZE: C · DRAWING NO. 60119300	REV: BT
		SHEET 244	5

DATA FLOW

In a read reference, the read word from the specified address flows from the storage modules to the data distributor and also back to the storage modules for restoration. The SE modules send the read word to the distributor and start the restore portion of the cycle. The restore FFs on these modules are cleared just before receiving the read word.

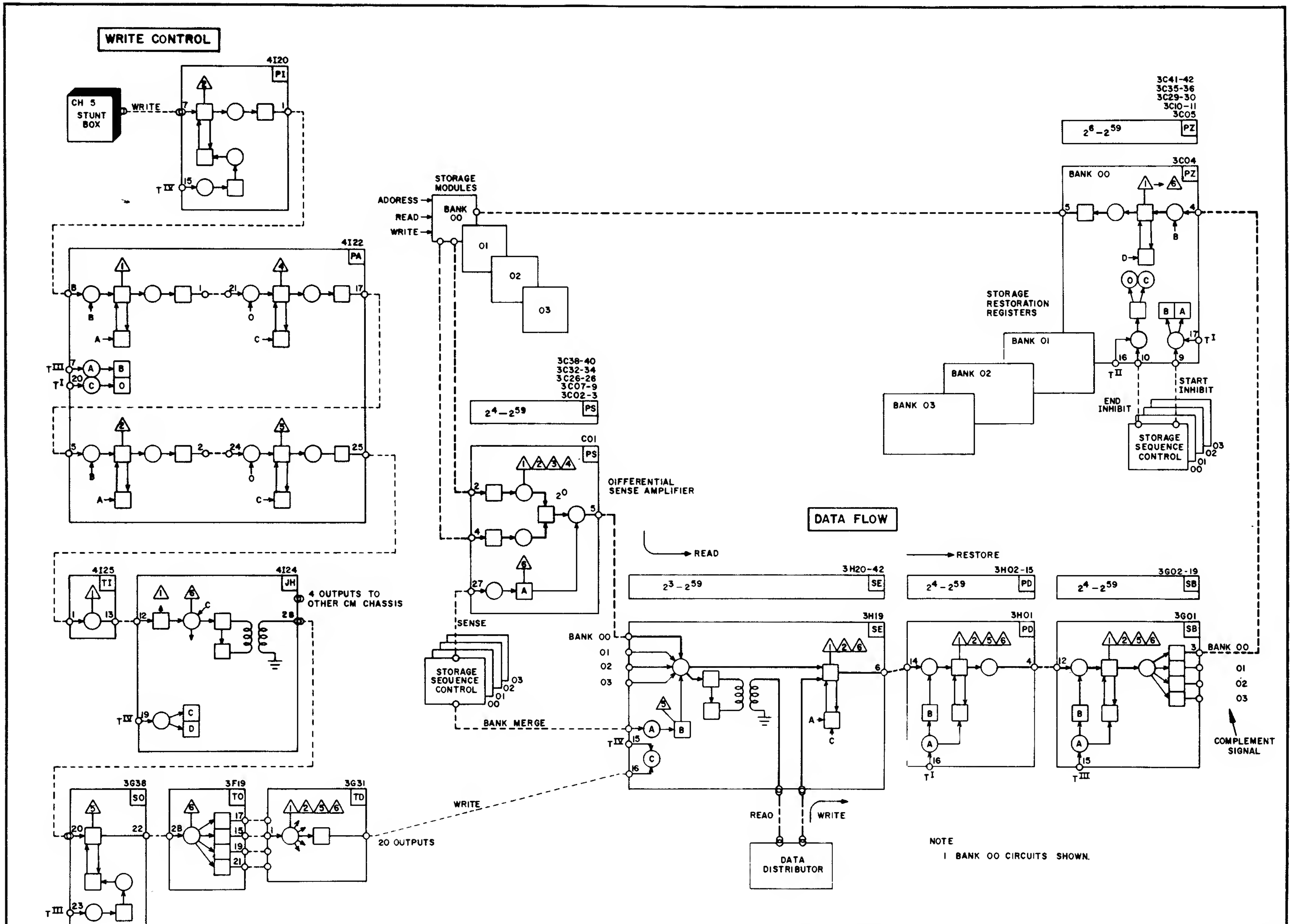
In a write reference, the read word from the specified address is sent to the data distributor and entered in the restore FFs of the SE modules. The restore FFs are cleared again to destroy the read word and reset with the write word which is stored in place of the read word during its normal restore cycle. The write control circuit and timing of stunt box tags direct the sequence.

WRITE CONTROL

Write control clears the restore FFs in the SE modules when writing in memory and thereby allows entry of the write word into the restore circuits.

A write signal from the stunt box enters the write control timing chain at the same time as the memory address is received in the input register of all memory chassis. The timing chain feeds a pulse to all chassis where they are fanned out and clear the restore FFs on the respective chassis SE modules. The delay time through the chain and format just exceeds the read access time and thereby destroys the read word immediately after it enters the SE restore FF. Effectively, the pulse in the timing chain runs in parallel with the pulse in the storage sequence control associated with the selected bank, but the write pulse from the timing chain fanout is emitted just after the bank merge pulse (which enters the read word in the SE restore FFs) from storage sequence control. Write pulses may enter the chain at minor cycle intervals and each is associated with a parallel operating storage sequence control.

The timing within the data distributor is such that a write word is sent to the SE modules slightly later than the SE modules send the read word to the data distributor.



CONTROL DATA CORPORATION	TITLE CENTRAL MEMORY (65K) DATA FLOW, WRITE CONTROL SERIALS 1-7	PRODUCT 6604	
COMPUTER DIVISION		SIZE C · DRAWING NO. 60119300	REV R
		SHEET 245	7

DATA DISTRIBUTOR

The data distributor distributes read and write words to and from CM. Read words are sent to CP control on chassis 5, CP registers on chassis 7 and 8, and to the PP on chassis 1.

Write words are accepted from CP control on chassis 5 (exchange jump or return jump instructions), CP register chassis 7 and 8 (X^{0-7} registers), or from the PP on chassis 1.

Address tags from the CP stunt box define the read or write cases and the origin or destination of the data.

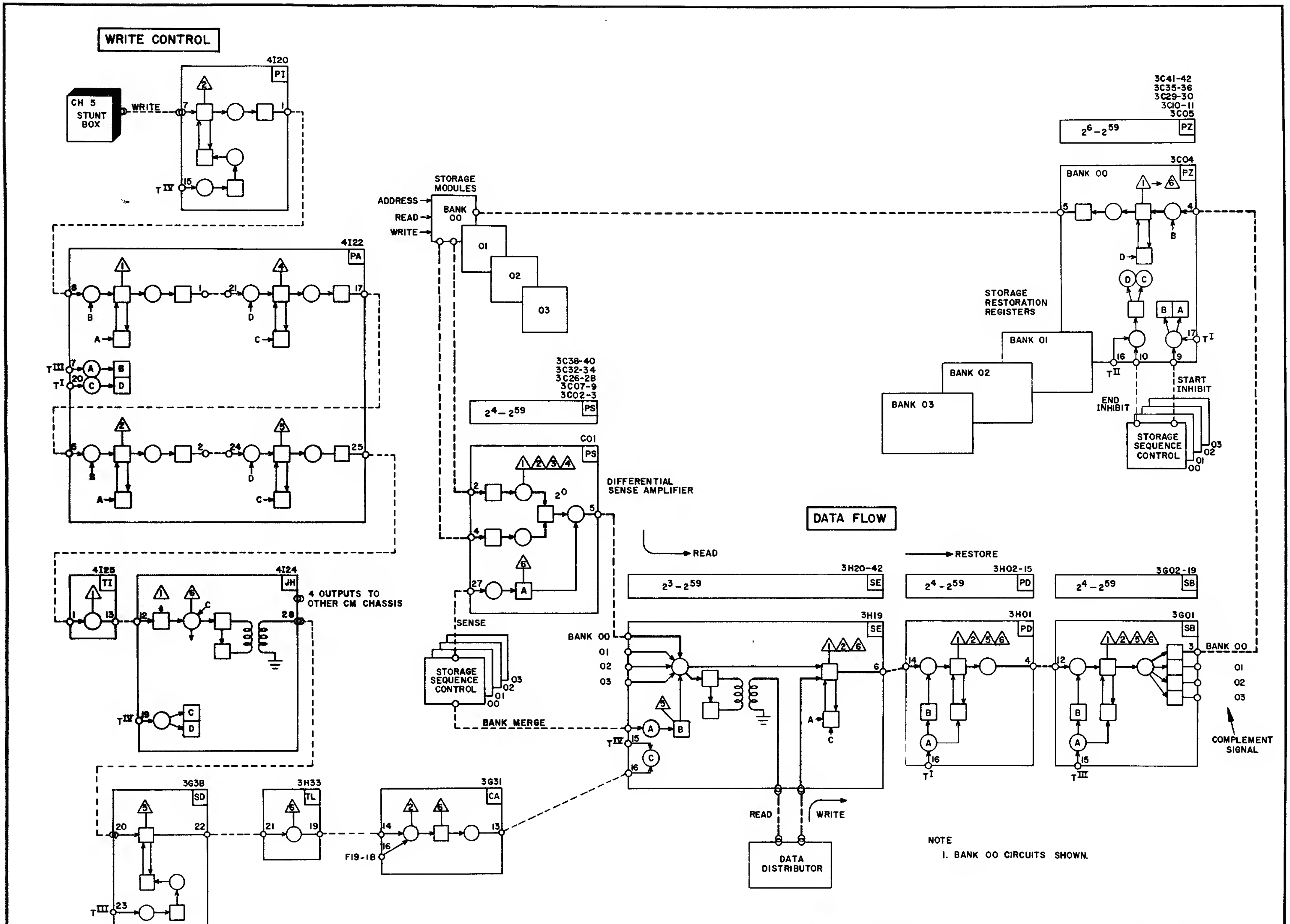
STORAGE CYCLE TIMING

Inhibit On and Off

The inhibit should turn on at least 20 nsec before the start of the Write, and stay on at least 15 nsec after the end of the Write. The inhibit time is measured on pin 5 of the PZ module and is compared to the Write on pin 24 of the PU module. It should not be necessary to adjust the on time for the inhibit 30-50 nsec is the usual delay between inhibit-on and write-on. The off time is adjusted by varying the length of wire to pin 14 of C21, F21, M21, or P21 (clock working ranks).

All of the preceding times are measured from the first crossing of the half amplitude point of the waveform. It is necessary that Change Order 14965 (6600) or 15349 (6400 and 6500) are installed prior to making any of the timing adjustments.

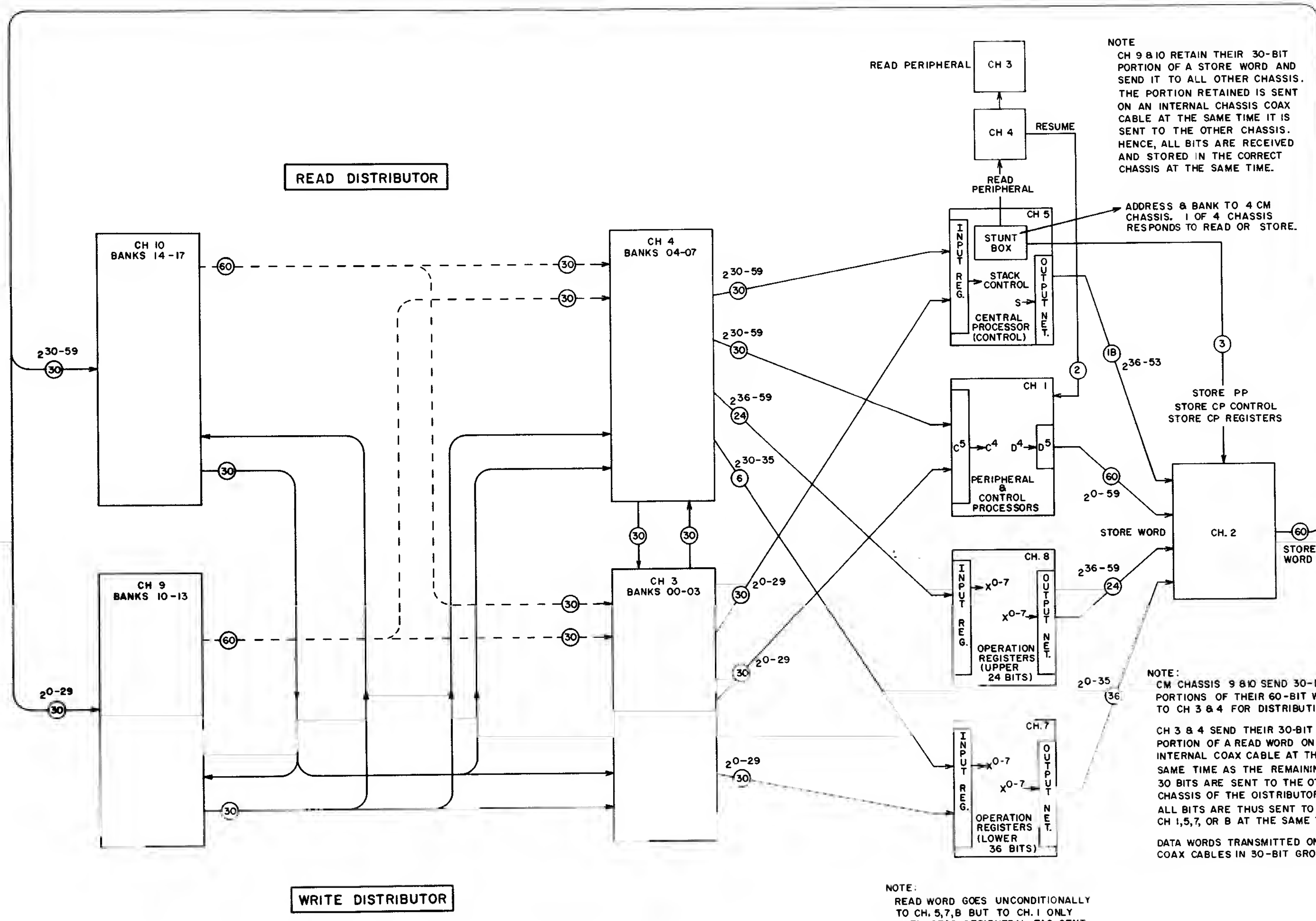
Use the SC module (test points 6, 4, 1, 3 for banks 0, 1, 2, 3) for the trigger source. It may not be possible to obtain a 395 nsec duration pulse for the read using the 180" wire called out in Change Order 14965 (6600 only). An additional change order has been written with a retrofit on failure. This change order just clears the read portion of the PU from a later time in the Storage Control Sequence. Change Order 17014 is applicable only to the 6600. The retrofit case changes the 180" wire from pin 24 of C15, F15, M15 or P15, to pin 26 of C16, F16, M16 or P16. The wire is then cut to the correct length to obtain 395 nsec ± 5 nsec.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
CENTRAL MEMORY (65K)
DATA FLOW, WRITE CONTROL
SERIALS 8-UP ONLY

PRODUCT	SIZE	DRAWING NO.	REV	SHEET	
6604/14	C	60119300	BF	272	8.1



NOTE
CH 9 & 10 RETAIN THEIR 30-BIT PORTION OF A STORE WORD AND SEND IT TO ALL OTHER CHASSIS. THE PORTION RETAINED IS SENT ON AN INTERNAL CHASSIS COAX CABLE AT THE SAME TIME IT IS SENT TO THE OTHER CHASSIS. HENCE, ALL BITS ARE RECEIVED AND STORED IN THE CORRECT CHASSIS AT THE SAME TIME.

NOTE:
CM CHASSIS 9 & 10 SEND 30-BIT PORTIONS OF THEIR 60-BIT WORD TO CH 3 & 4 FOR DISTRIBUTION.

CH 3 & 4 SEND THEIR 30-BIT PORTION OF A READ WORD ON AN INTERNAL COAX CABLE AT THE SAME TIME AS THE REMAINING 30 BITS ARE SENT TO THE OTHER CHASSIS OF THE DISTRIBUTOR ALL BITS ARE THUS SENT TO CH 1,5,7, OR 8 AT THE SAME TIME.

DATA WORDS TRANSMITTED ON COAX CABLES IN 30-BIT GROUPS.

NOTE:
READ WORD GOES UNCONDITIONALLY TO CH. 5,7,8 BUT TO CH. 1 ONLY WHEN READ PERIPHERAL TAG SENT.

NOTE:
ALL LINES ARE COAXIAL CABLES.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY (65K) DATA DISTRIBUTOR	PRODUCT 6604 SIZE C · DRAWING NO 60119300 · REV K SHEET 246 · PAGE 9

The read distributor accepts read words from the 4 CM chassis and routes them to the several destinations.

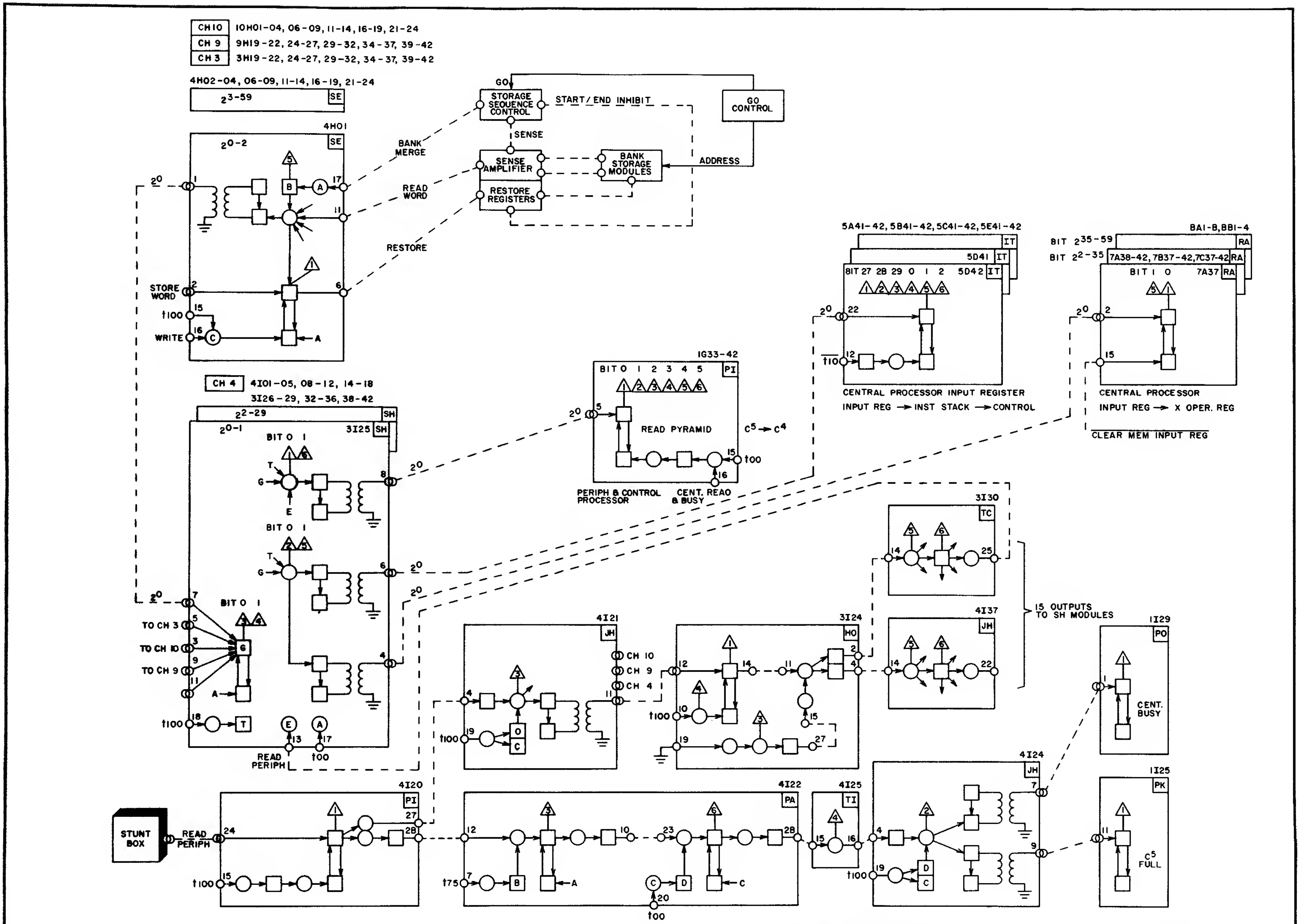
The distributor is organized on chassis 3 and 4, each of which handles 30 bits of the 60-bit word. Chassis cable limitations dictate the organization. The listing below shows the bits handled by each chassis.

CHASSIS	BITS
3	0-29
4	30-59

Chassis 9-10 each send the same 30-bit group to chassis 3, and 4. A read word from chassis 3 retains bits 0-29 but sends remaining bits to chassis 4. Read words from chassis 4 are handled similarly. Intra-chassis coaxial cables are used on chassis 3 and 4 for their 30-bit portions so that timing is consistent with the chassis receiving the data.

Each read word is sent unconditionally from chassis 3 and 4 to chassis 5 (CP control) and chassis 7 and 8 (CP registers). A read peripheral tag from the stunt box is sent to chassis 4 and then on to chassis 3. The tag gates the read word to the C^5 register in the read pyramid on PP chassis 1.

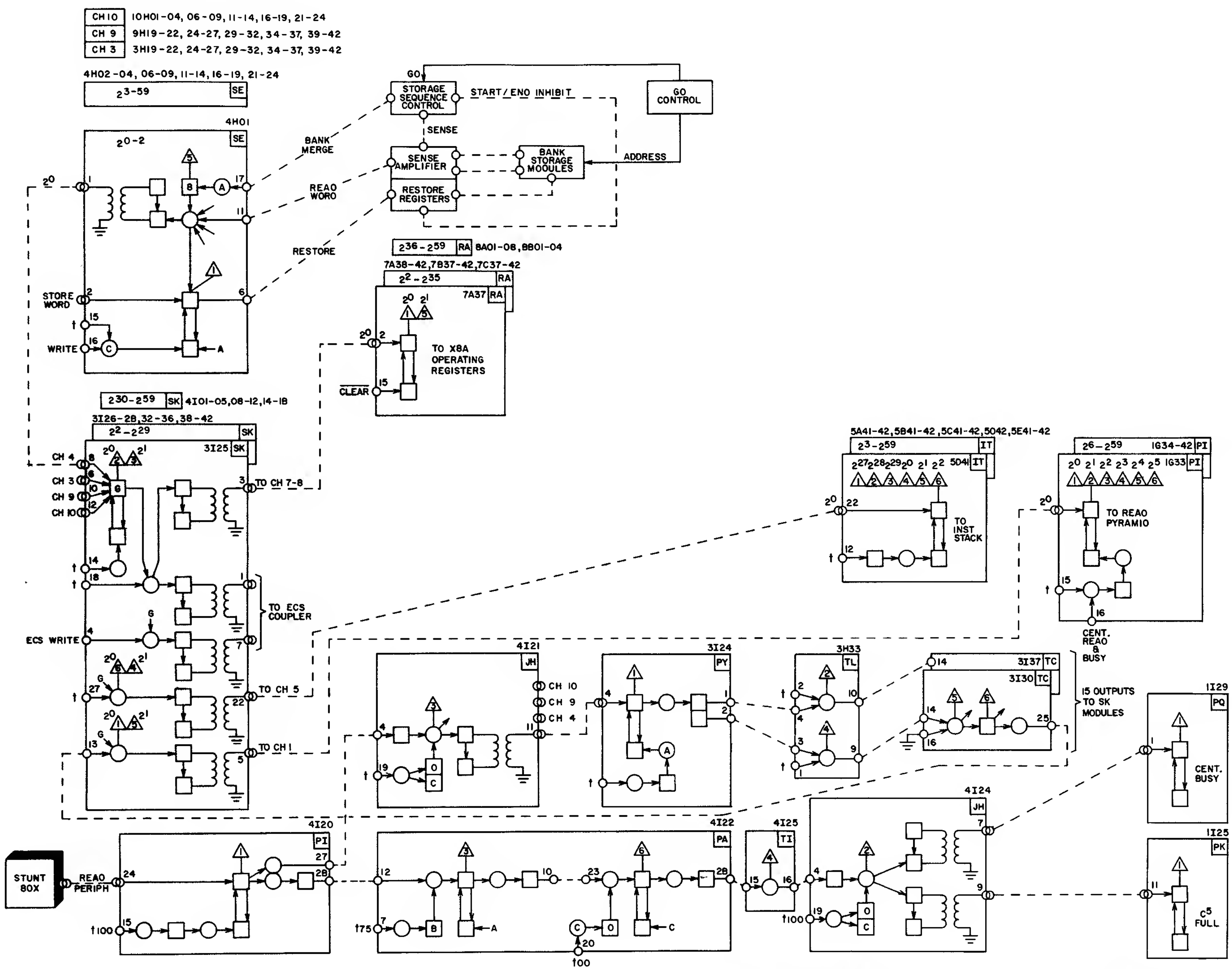
The read peripheral tag also enters a time delay chain and is returned to the PP as a resume signal. The resume sets the C^5 full FF in the PP (after data word is in C^5) to signal the presence of the read word. The same resume also clears the central busy FF to indicate to PP control that the address has been accepted by the stunt box and CM has delivered the word. This allows the PPs to proceed and send another address to the stunt box.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE: CENTRAL MEMORY (65K) READ DISTRIBUTOR SERIALS 1-7

PRODUCT	SIZE	DRAWING NO.	REV	SHEET	PAGE
6604	C	60119300	M	247	11



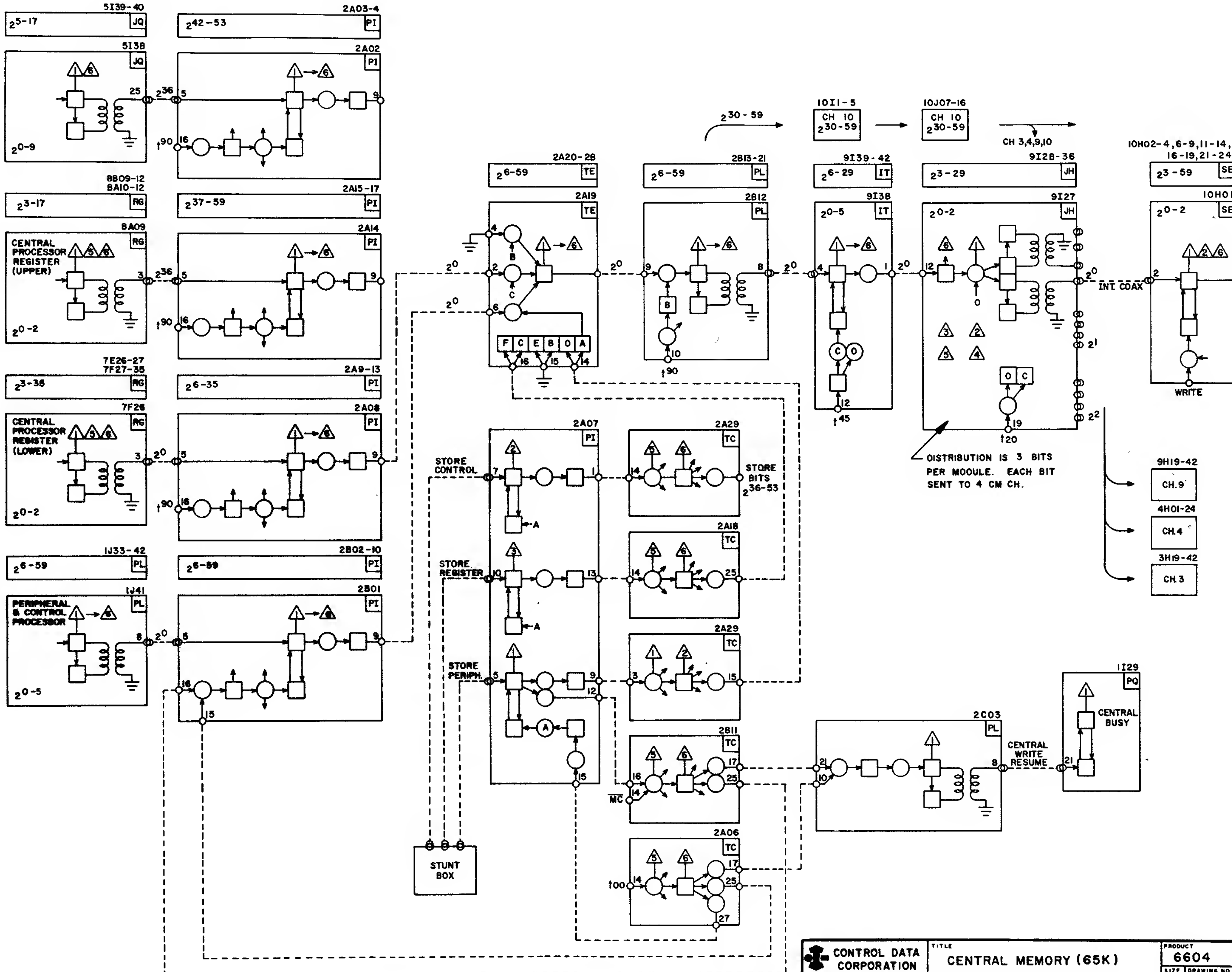
CONTROL DATA CORPORATION	TITLE	PRODUCT 6604/14
COMPUTER DIVISION	CENTRAL MEMORY (65K) READ DISTRIBUTOR SERIALS 8-UP	SIZE C · DRAWING NO. 60119300 · REV P · SHEET 265 · PAGE 12.1

WRITE DISTRIBUTOR

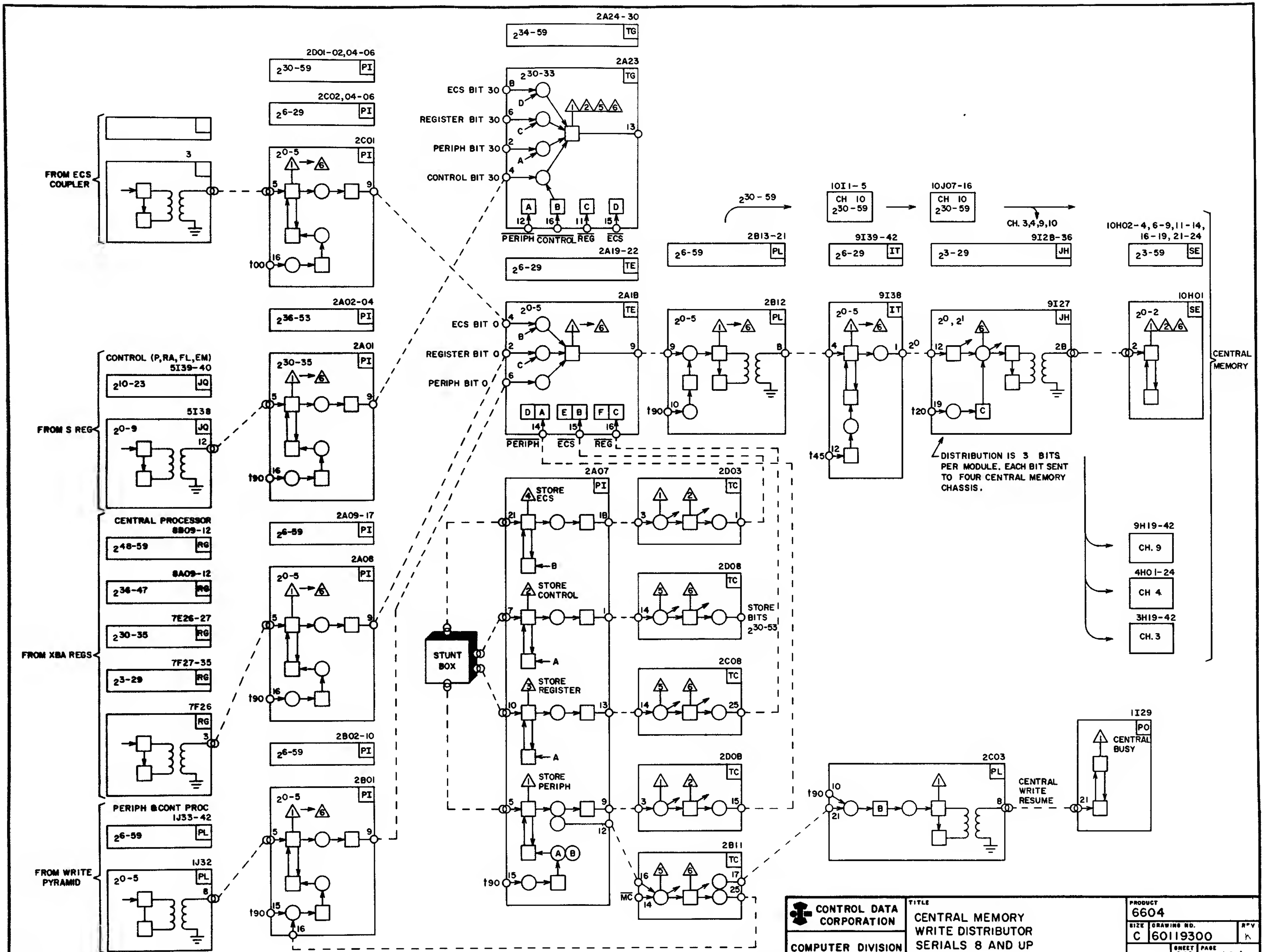
The write distributor accepts words from the several sources and stores them in 1 of 4 memory chassis. The distributor is on chassis 2. The 60-bit word on chassis 2 is split into two 30-bit groups which are sent to chassis 9-10 respectively. Each of these chassis in turn sends (or stores) its 30-bit group to the other 2 chassis unconditionally.

A 3-to-1 fan-in on chassis 2 selects the proper word under control of the store tag from the stunt box which is established ahead of the data. The word is then split and transmitted to chassis 9-10. The chassis 2 data registers and the tag FFs are cleared simultaneously.

One minor cycle after the register clear, a central write resume is sent to the PP to clear the central busy FF and allow the PPs to send another address to the stunt box.



CONTROL DATA CORPORATION	TITLE: CENTRAL MEMORY (65K) WRITE DISTRIBUTOR SERIALS 1-7	PRODUCT: 6604	
COMPUTER DIVISION		SIZE: C / DRAWING NO.: 60119300 / REV: K	SHEET 248 / 13



CONTROL DATA CORPORATION

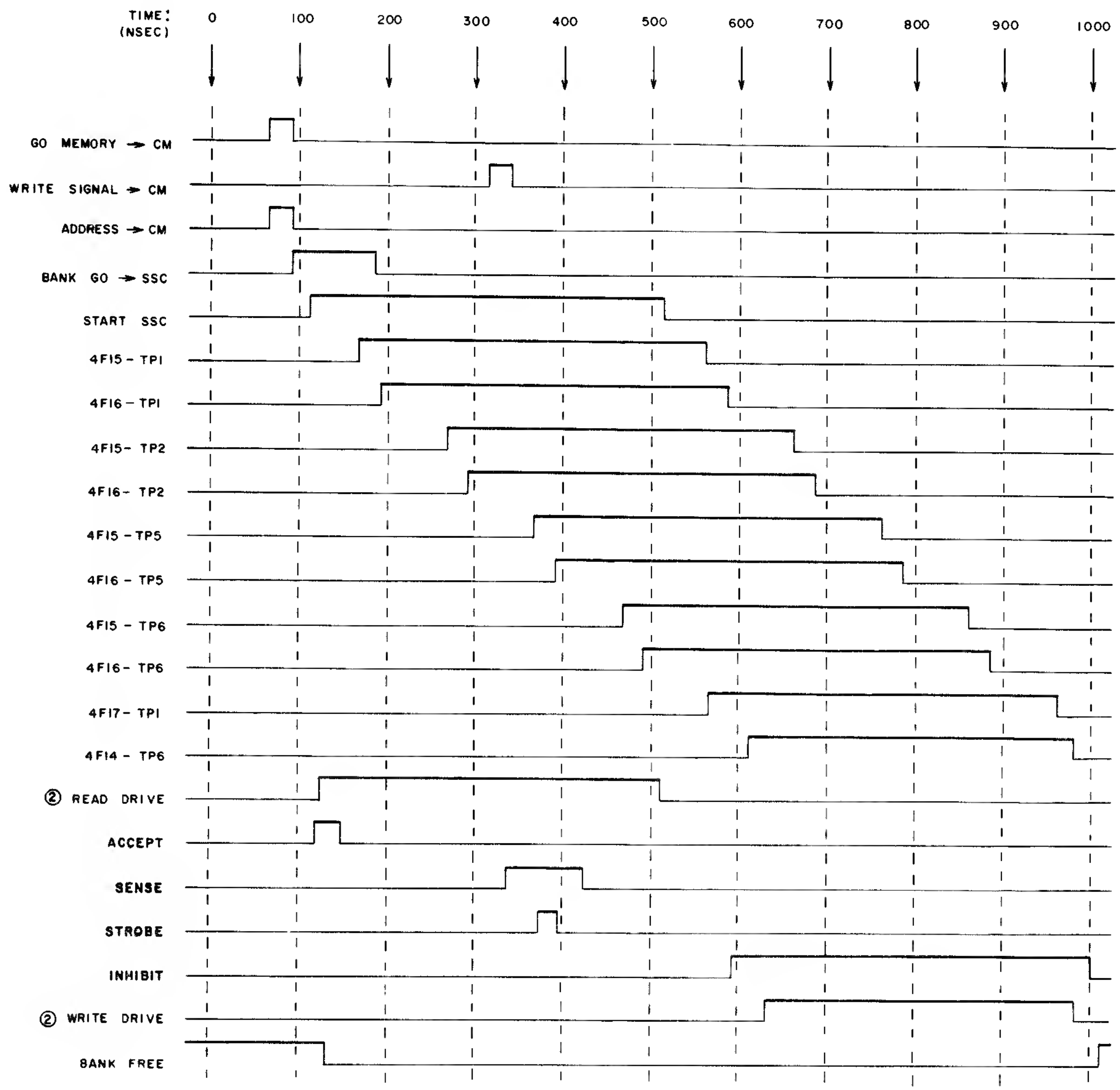
COMPUTER DIVISION

TITLE: CENTRAL MEMORY WRITE DISTRIBUTOR SERIALS 8 AND UP

PRODUCT 6604

SIZE C | DRAWING NO. 60119300 | REV

SHEET 249 | PAGE 14.1



NOTES:

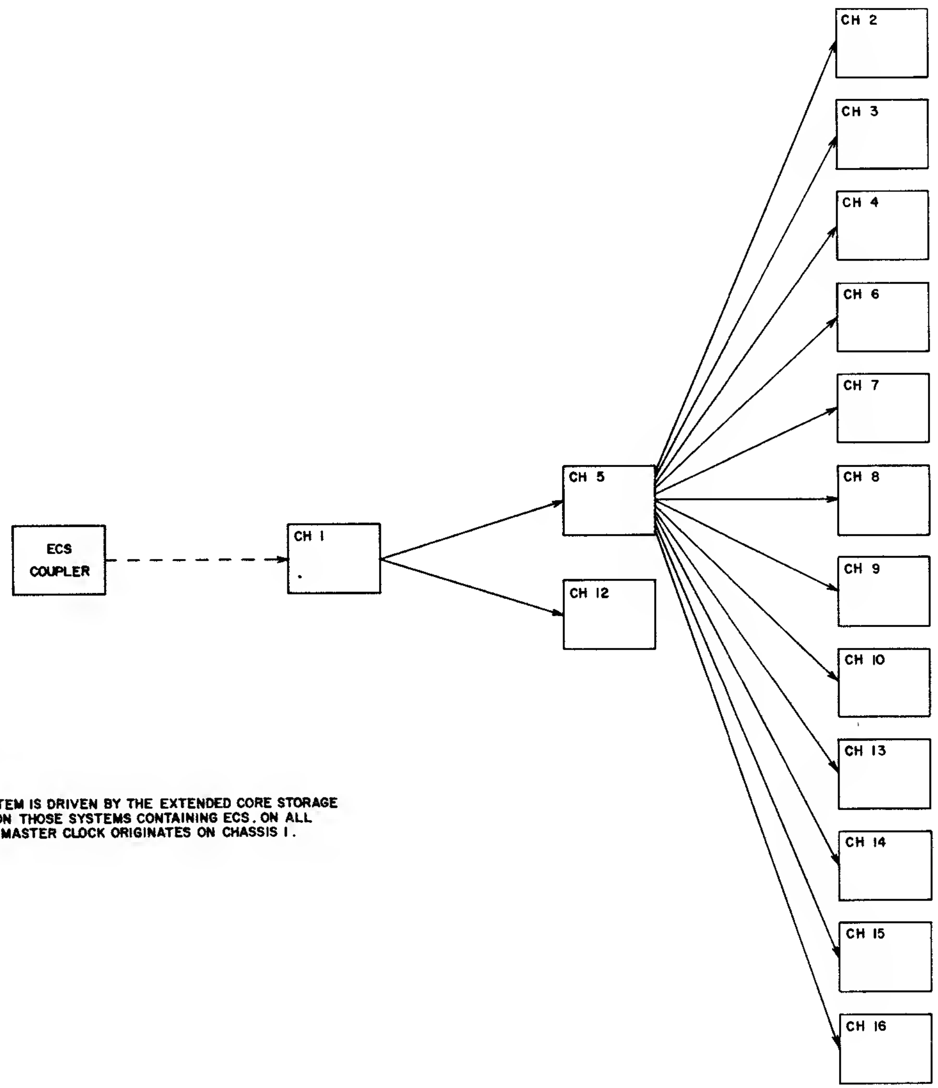
1. STORAGE CYCLE TIMING IS TYPICAL FOR ALL MEMORY CHASSIS (CHASSIS 4, BANK 00 LOCATIONS AND TP'S SHOWN).
2. READ/WRITE DRIVE TIMES SHOWN ARE THAT OF OUTPUT PINS ON 4F14

THIS SHEET IS IDENTICAL TO CENTRAL MEMORY (65K) PAGE 15

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: CENTRAL MEMORY STORAGE CYCLE TIMING	PRODUCT: 6601/04; SIZE: C; DRAWING NO: 60119300; REV: BT; SHEET: 45; PAGE: 15

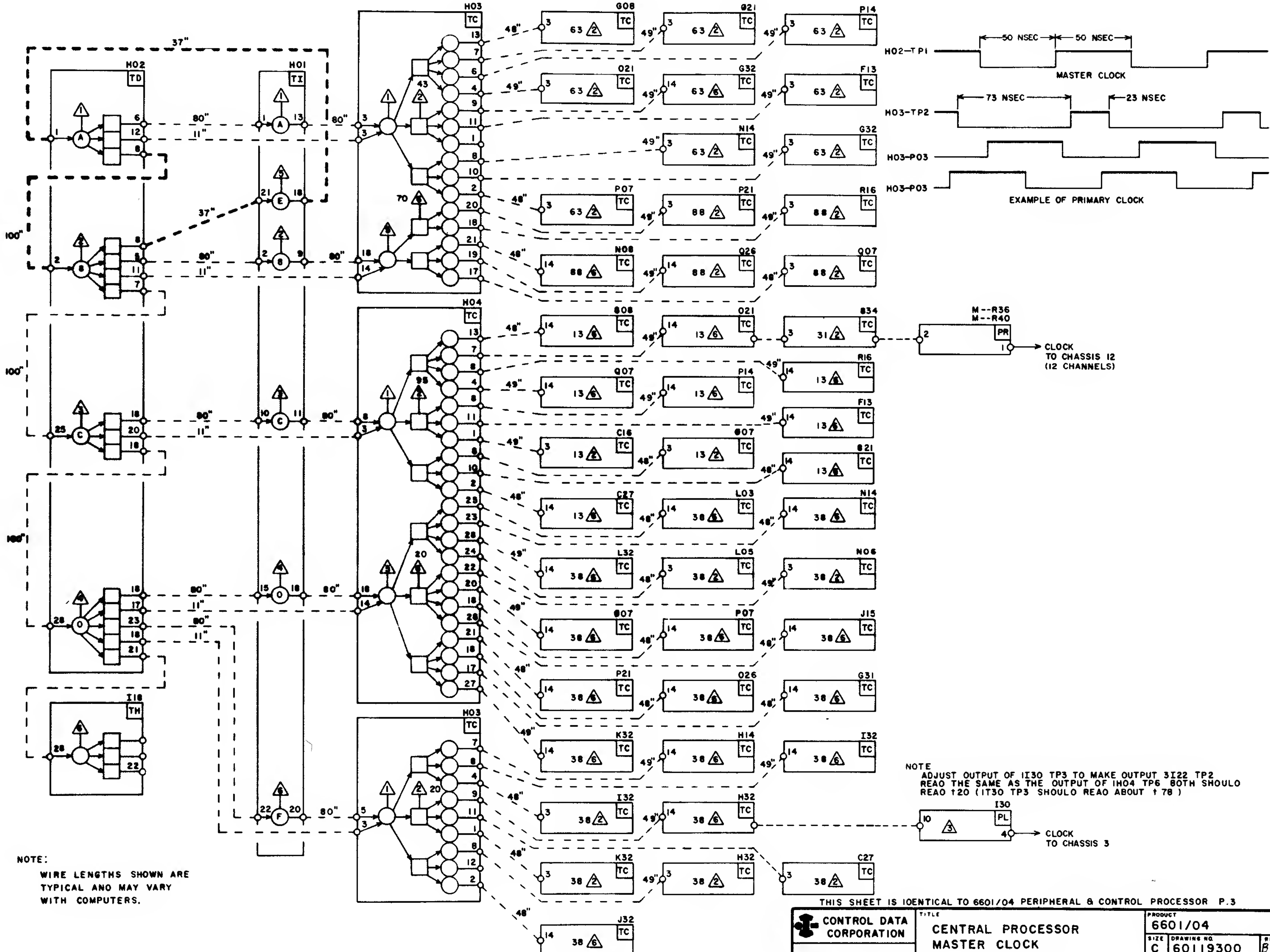
CLOCK

CONTENTS



NOTE :
THE 6600 CLOCK SYSTEM IS DRIVEN BY THE EXTENDED CORE STORAGE (ECS) COUPLER ONLY ON THOSE SYSTEMS CONTAINING ECS. ON ALL OTHER SYSTEMS, THE MASTER CLOCK ORIGINATES ON CHASSIS 1.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL COMPUTER CLOCK SYSTEM	PRODUCT 6601/04/13/14 SIZE C DRAWING NO. 60119300 REV M SHEET 115 PAGE 1

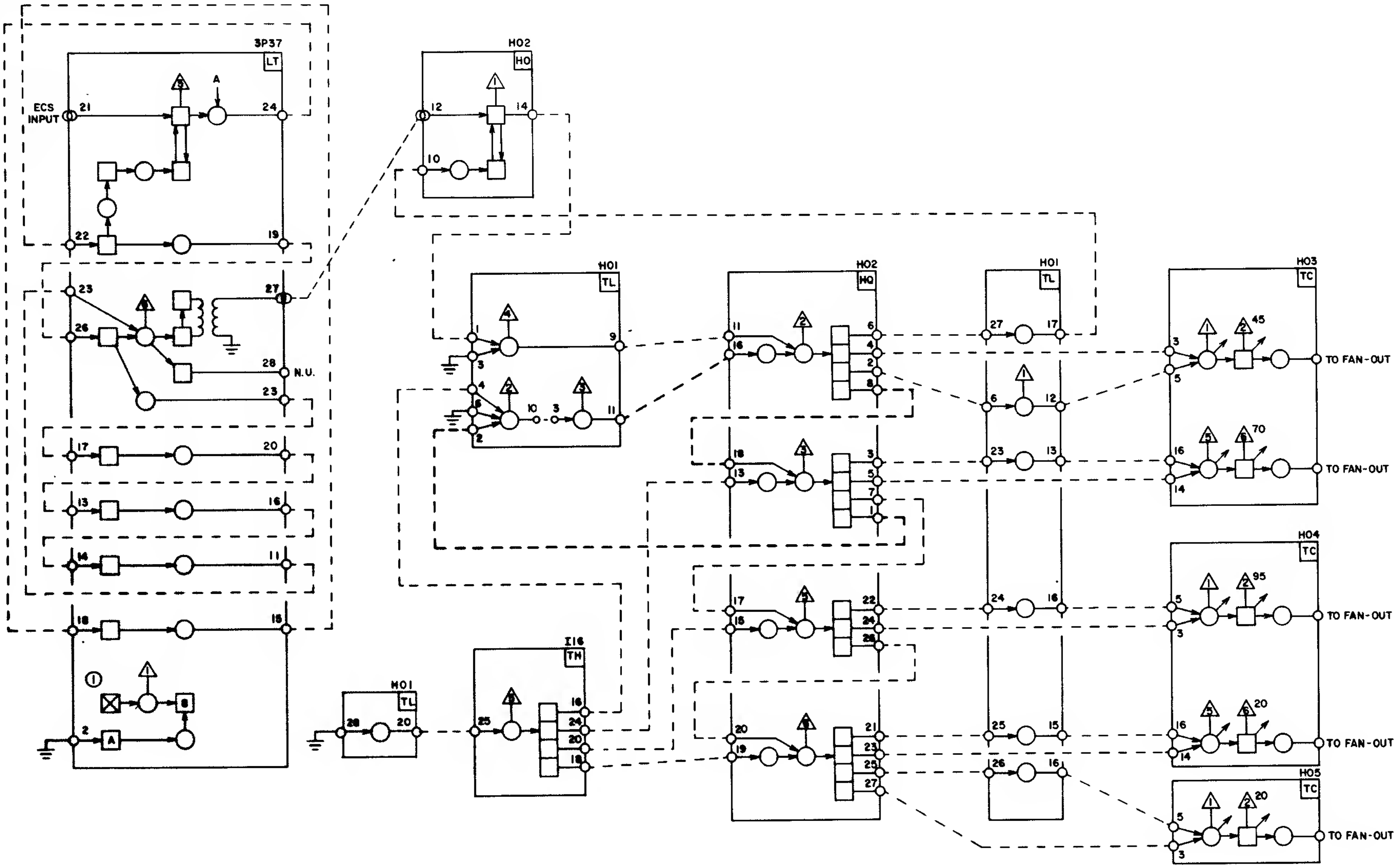


NOTE
ADJUST OUTPUT OF I130 TP3 TO MAKE OUTPUT 3I22 TP2 READ THE SAME AS THE OUTPUT OF IH04 TP6 BOTH SHOULD READ †20 (I130 TP3 SHOULD READ ABOUT † 78)

NOTE:
WIRE LENGTHS SHOWN ARE TYPICAL AND MAY VARY WITH COMPUTERS.

THIS SHEET IS IDENTICAL TO 6601/04 PERIPHERAL & CONTROL PROCESSOR P.3

CONTROL DATA CORPORATION	TITLE CENTRAL PROCESSOR MASTER CLOCK CHASSIS 1 SERIALS 1-7	PRODUCT 6601/04	
COMPUTER DIVISION		SIZE C	DRAWING NO. 60119300 REV BK
		SHEET 116	3

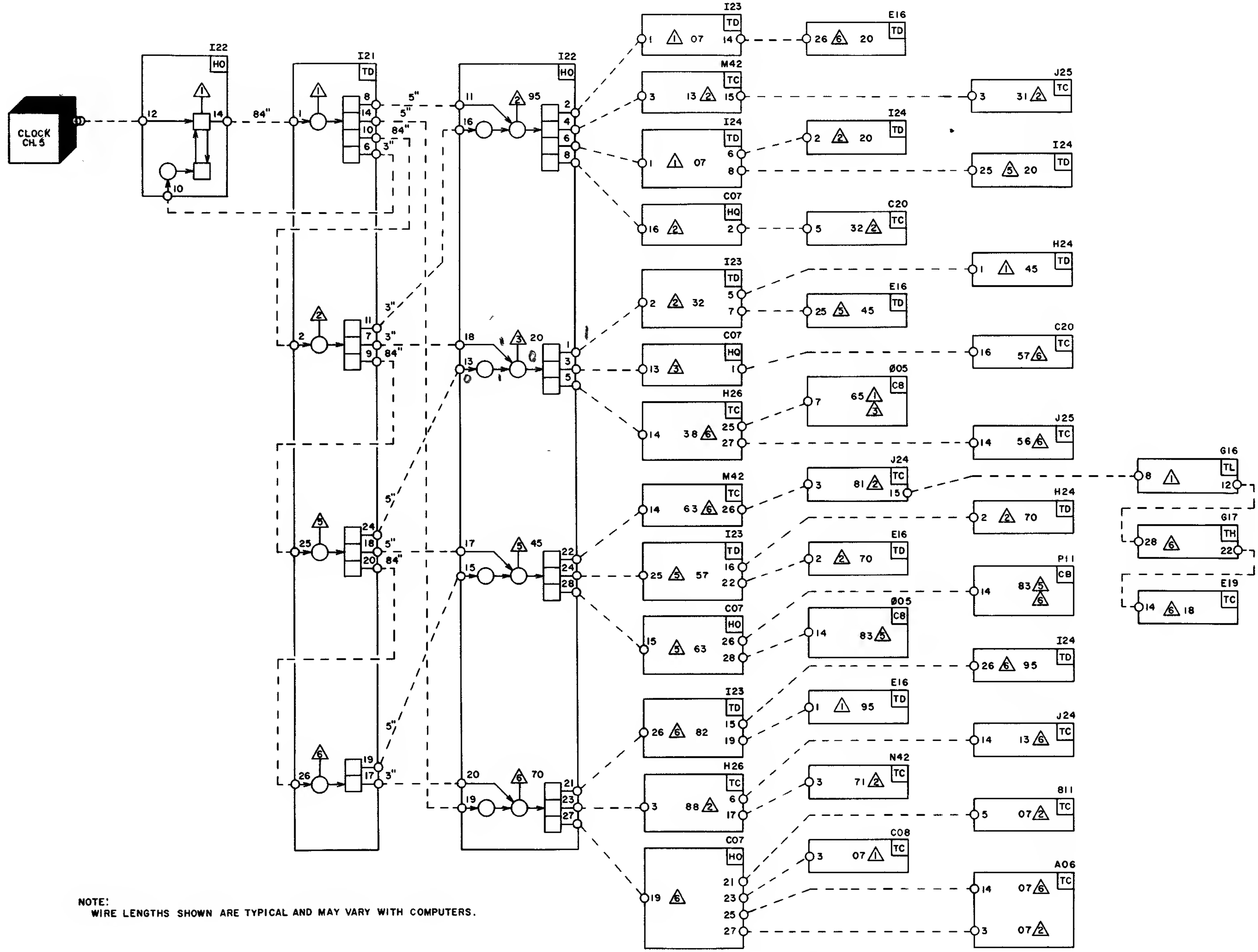


NOTES:

1 ☒ = CRYSTAL OSCILLATOR CIRCUIT USING 10 MHz CRYSTAL.

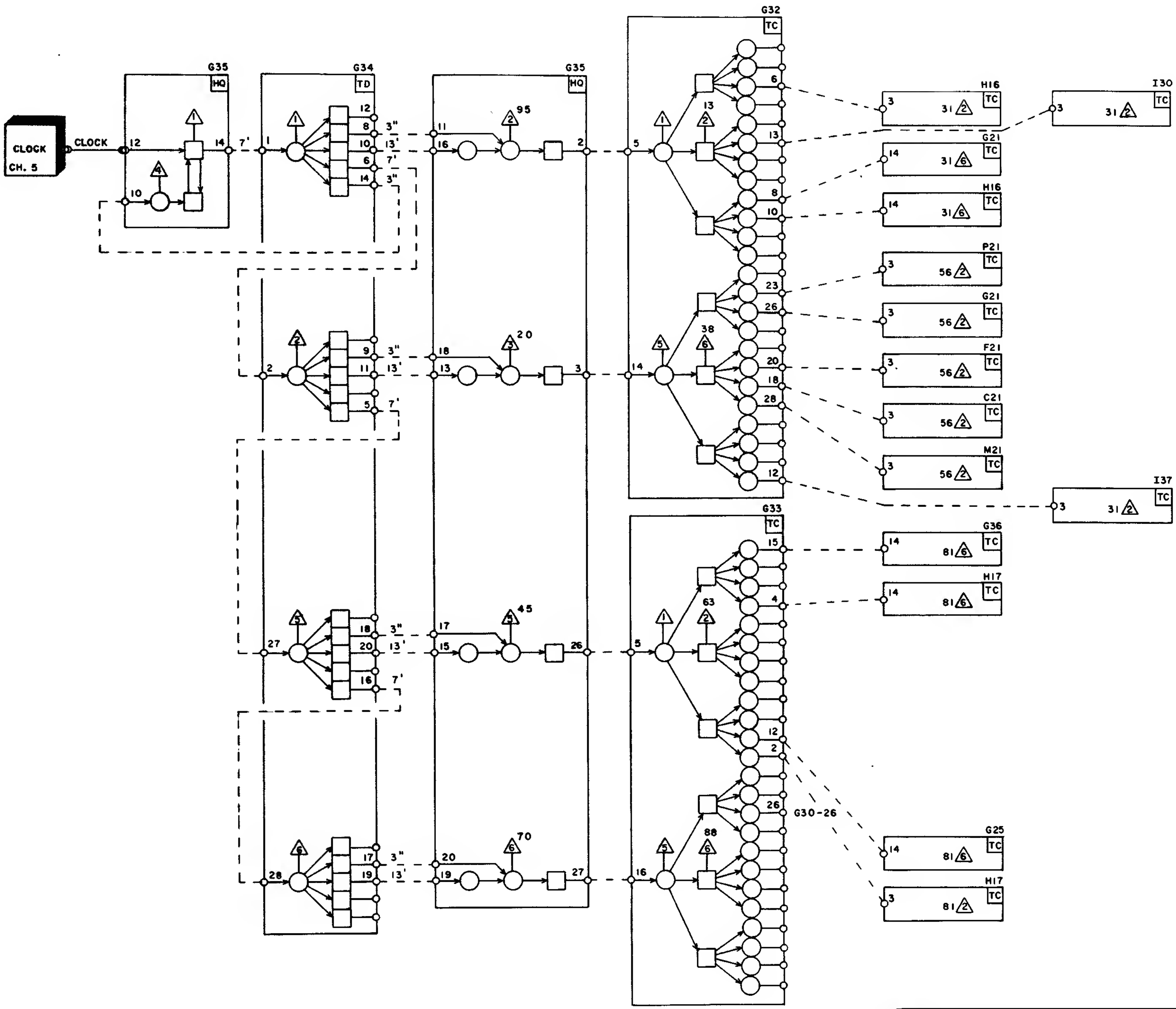
2 TURN TO PAGE 5 FOR COMPLETE CLOCK FAN-OUT ON CHASSIS 1

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL PROCESSOR MASTER CLOCK CHASSIS 1, SERIALS 8-UP	PRODUCT 6601/04/13/14 SIZE C · DRAWING NO. 60119300 · REV BT	SHEET 267 · 4.1

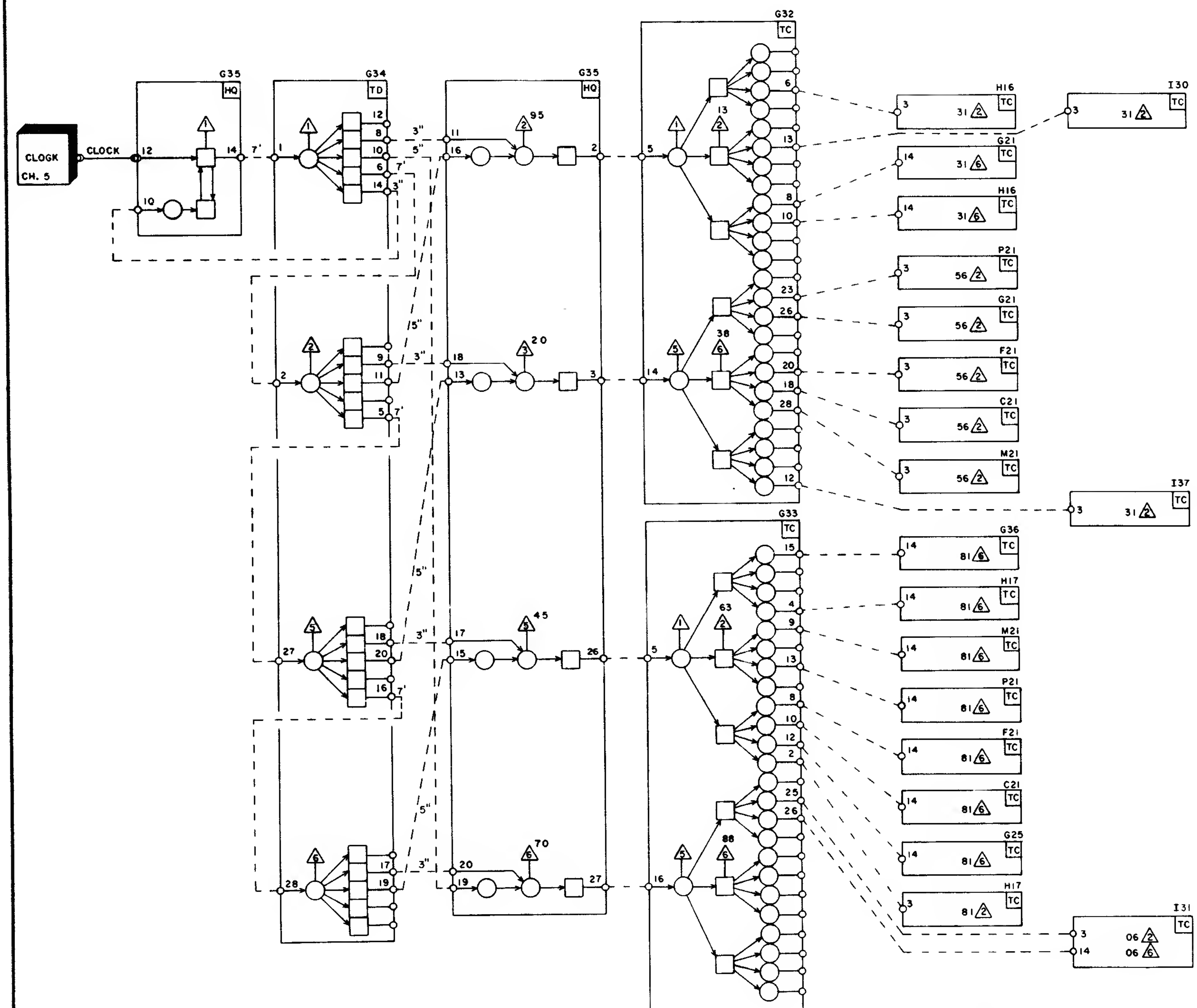


NOTE:
WIRE LENGTHS SHOWN ARE TYPICAL AND MAY VARY WITH COMPUTERS.

CONTROL DATA CORPORATION / COMPUTER DIVISION	TITLE: CENTRAL PROCESSOR CLOCK CH. 2	PRODUCT 6601/04
SIZE C	DRAWING NO. 60119300	REV BT
SHEET 117	PAGE 5	



CONTROL DATA CORPORATION	TITLE	PRODUCT 6601/04	
COMPUTER DIVISION	CENTRAL MEMORY CLOCK CH. 3, 9, 13, 15	SIZE C	DRAWING NO. 60119300
		SHEET 118	REV BT
		7.1	



CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE: CENTRAL MEMORY CLOCK
CH. 3,9,13,15
SERIALS 32 AND UP ONLY

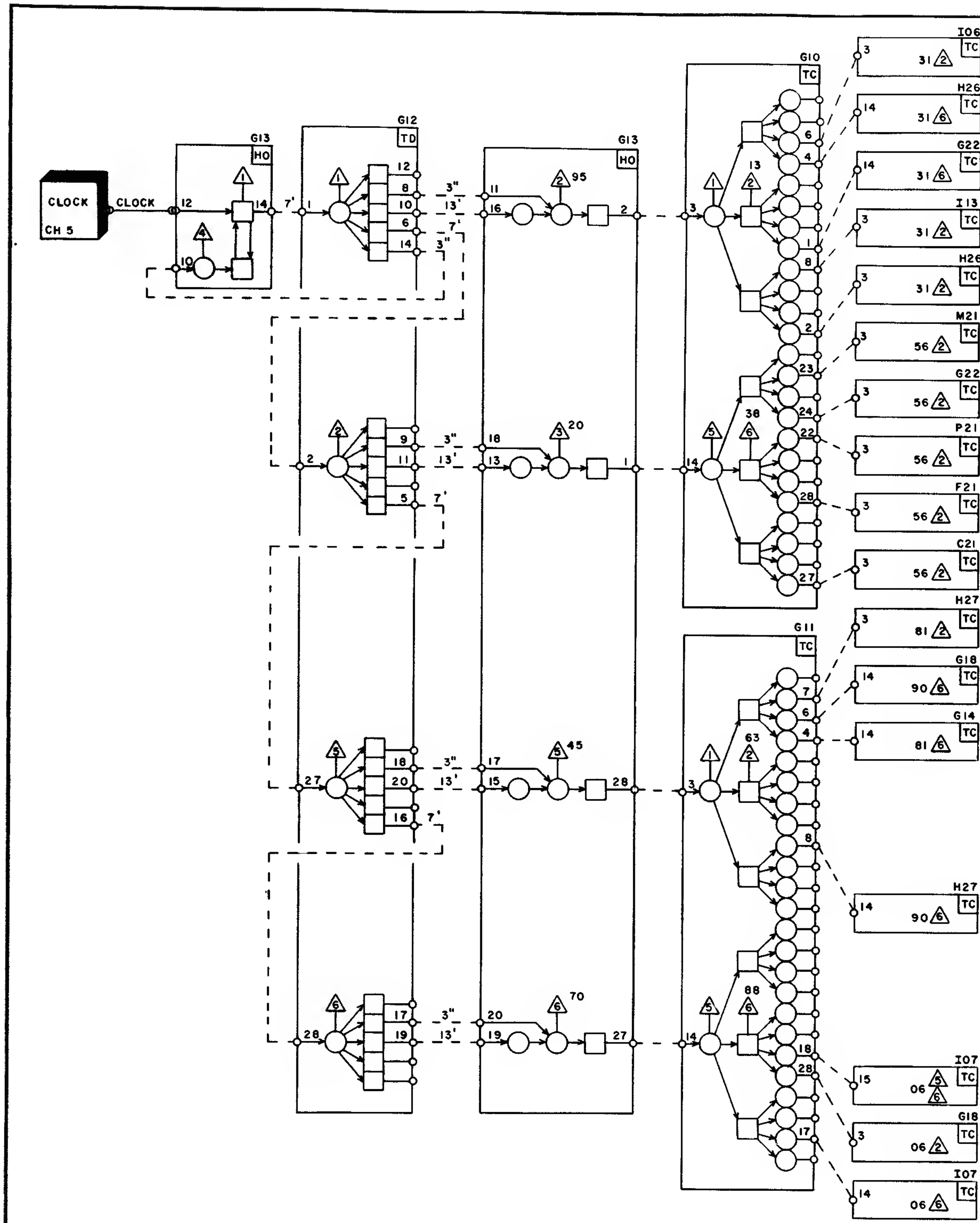
PRODUCT: 6601/04

SIZE: C

DRAWING NO: 60119300

SHEET: 118

7.3



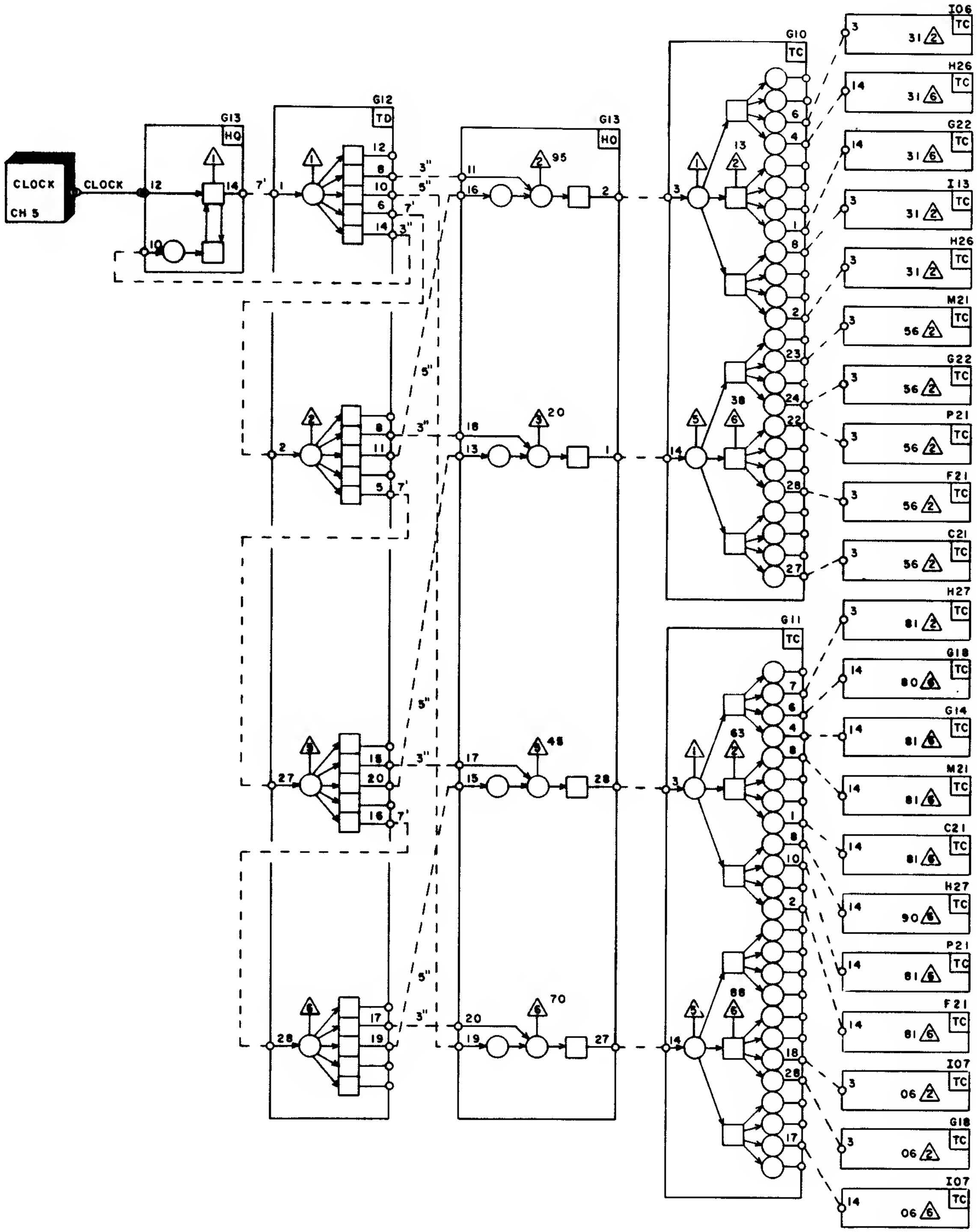
CONTROL DATA CORPORATION

COMPUTER DIVISION

TITLE

CENTRAL MEMORY
CLOCK
CH. 4,10,14,16

PRODUCT		
6601/04		
SIZE C	DRAWING NO 60119300	REV BT
	SHEET 119	9.1



CONTROL DATA CORPORATION

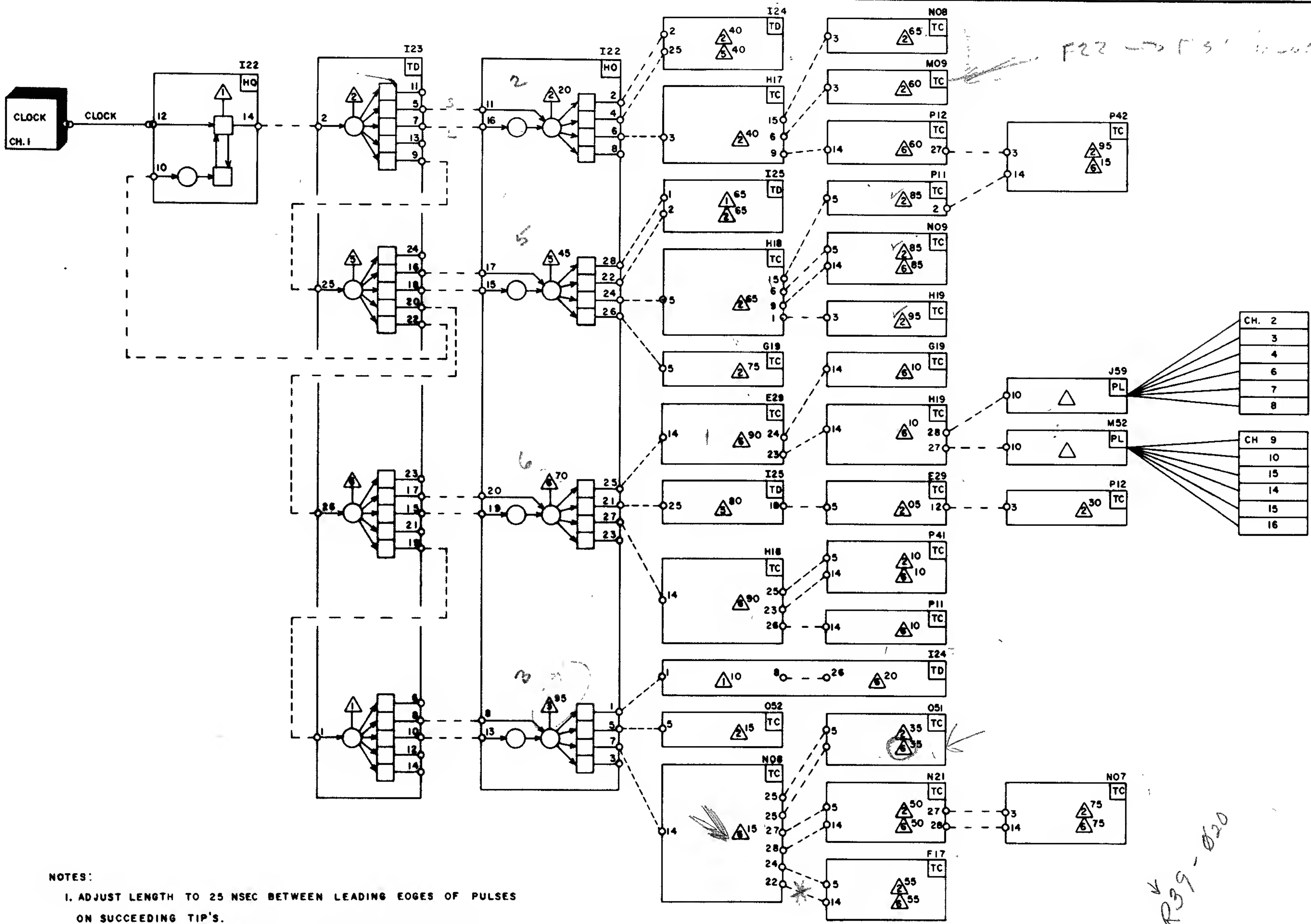
COMPUTER DIVISION

TITLE: CENTRAL MEMORY CLOCK
CH. 4, 10, 14, 16
SERIALS 32 AND UP ONLY

PRODUCT 6601/04

SIZE C | DRAWING NO. 60119300 | REV

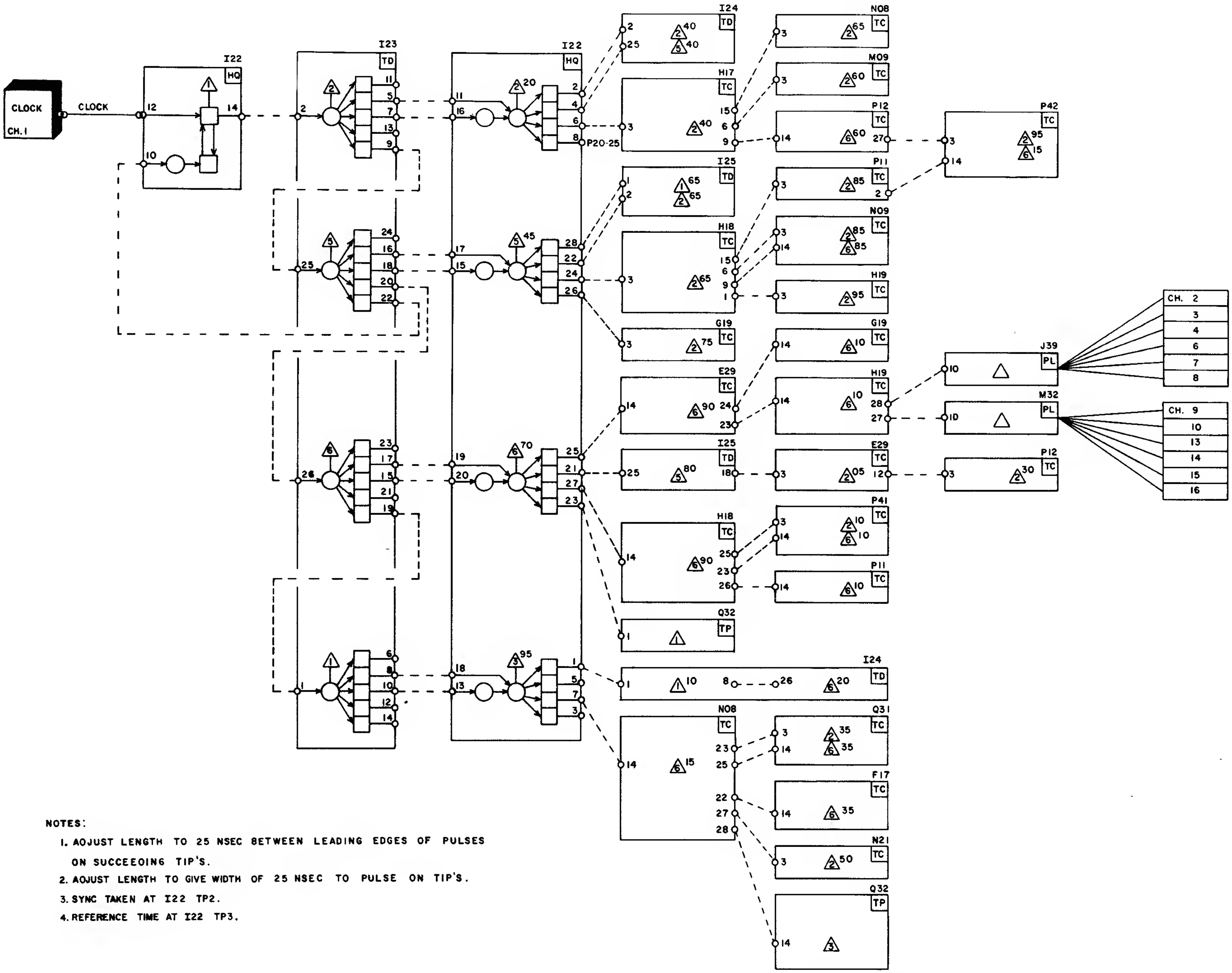
SHEET 119 | 9.3



NOTES:

1. ADJUST LENGTH TO 25 NSEC BETWEEN LEADING EDGES OF PULSES ON SUCCEEDING TIP'S.
2. ADJUST LENGTH TO GIVE WIDTH OF 25 NSEC TO PULSE ON TIP'S.
3. SYNC TAKEN AT I22 TP2.
4. REFERENCE TIME AT I22 TP5.

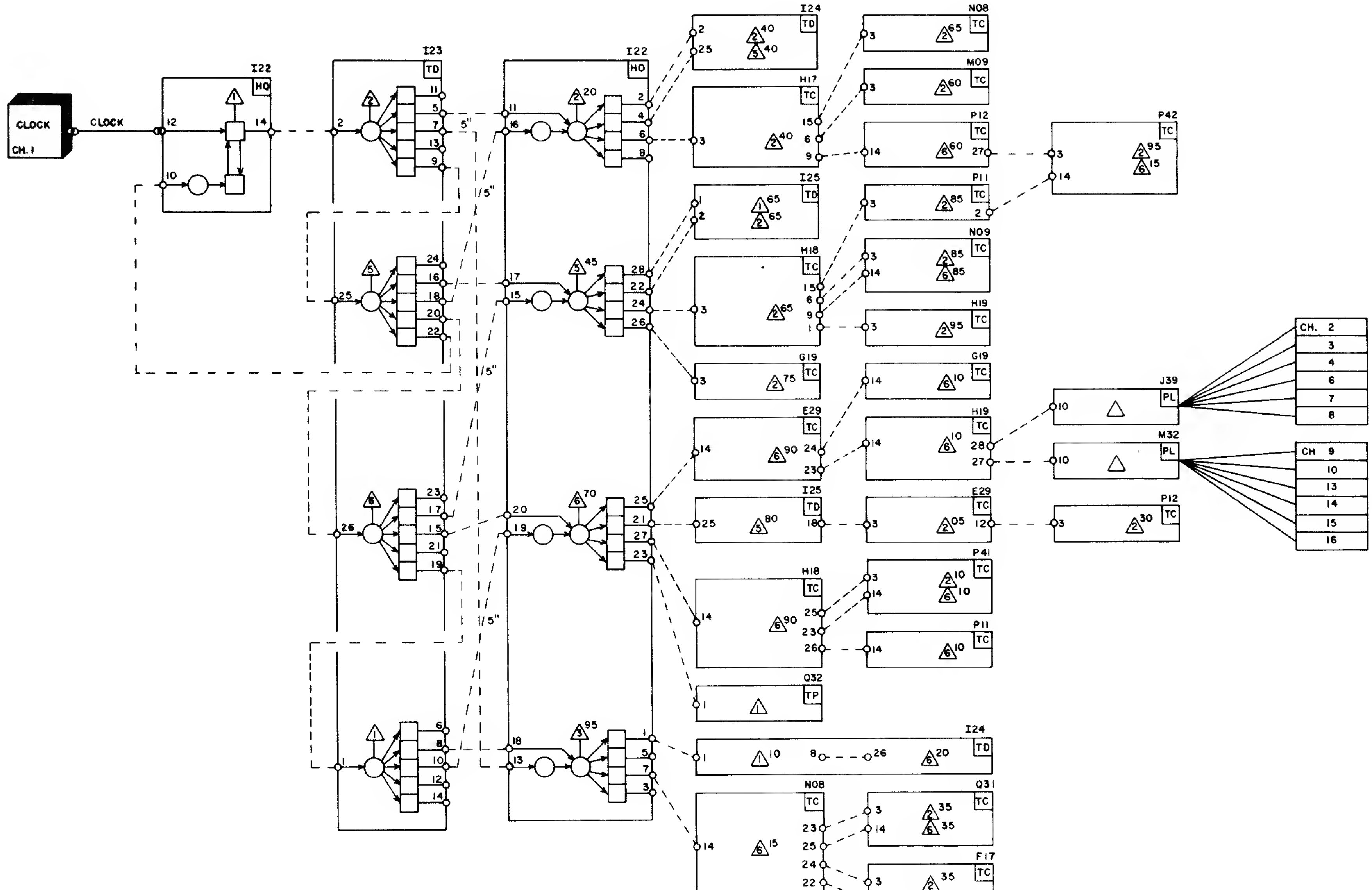
CONTROL DATA CORPORATION	TITLE: CENTRAL PROCESSOR CLOCK CH. 5 (SERIALS 1-7)	PRODUCT: 6601/04	
COMPUTER DIVISION		SIZE: C · DRAWING NO: 60119300 · SHEET: 120	REV: M · 11



NOTES:

1. ADJUST LENGTH TO 25 NSEC BETWEEN LEADING EDGES OF PULSES ON SUCCEEDING TIP'S.
2. ADJUST LENGTH TO GIVE WIDTH OF 25 NSEC TO PULSE ON TIP'S.
3. SYNC TAKEN AT I22 TP2.
4. REFERENCE TIME AT I22 TP3.

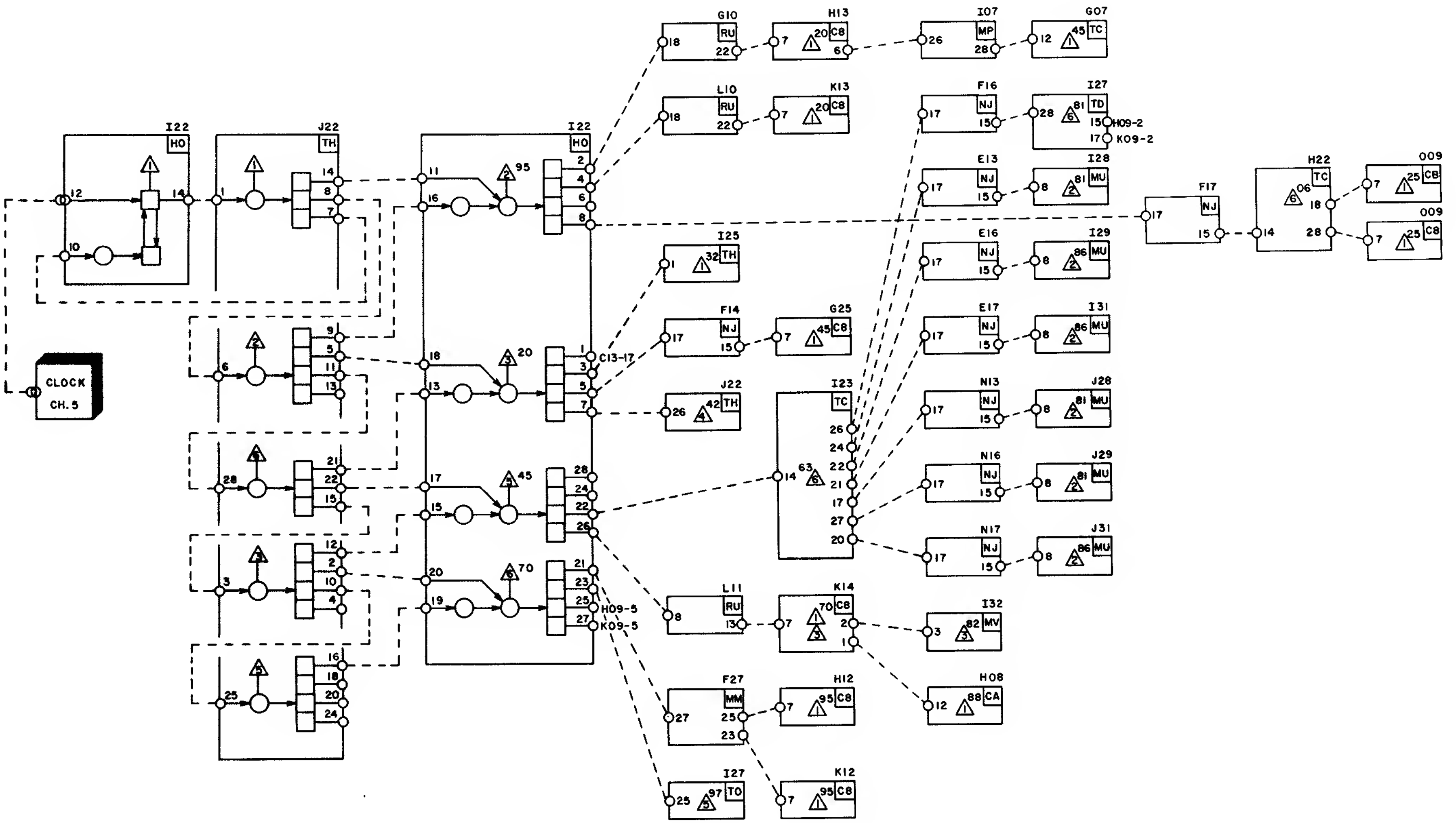
CONTROL DATA CORPORATION	TITLE CENTRAL PROCESSOR CLOCK CH. 5, SERIALS 8-31	PRODUCT 6601/04/13/14	
COMPUTER DIVISION		SIZE C	DRAWING NO 60119300 REV BT
		SHEET 273	12.1



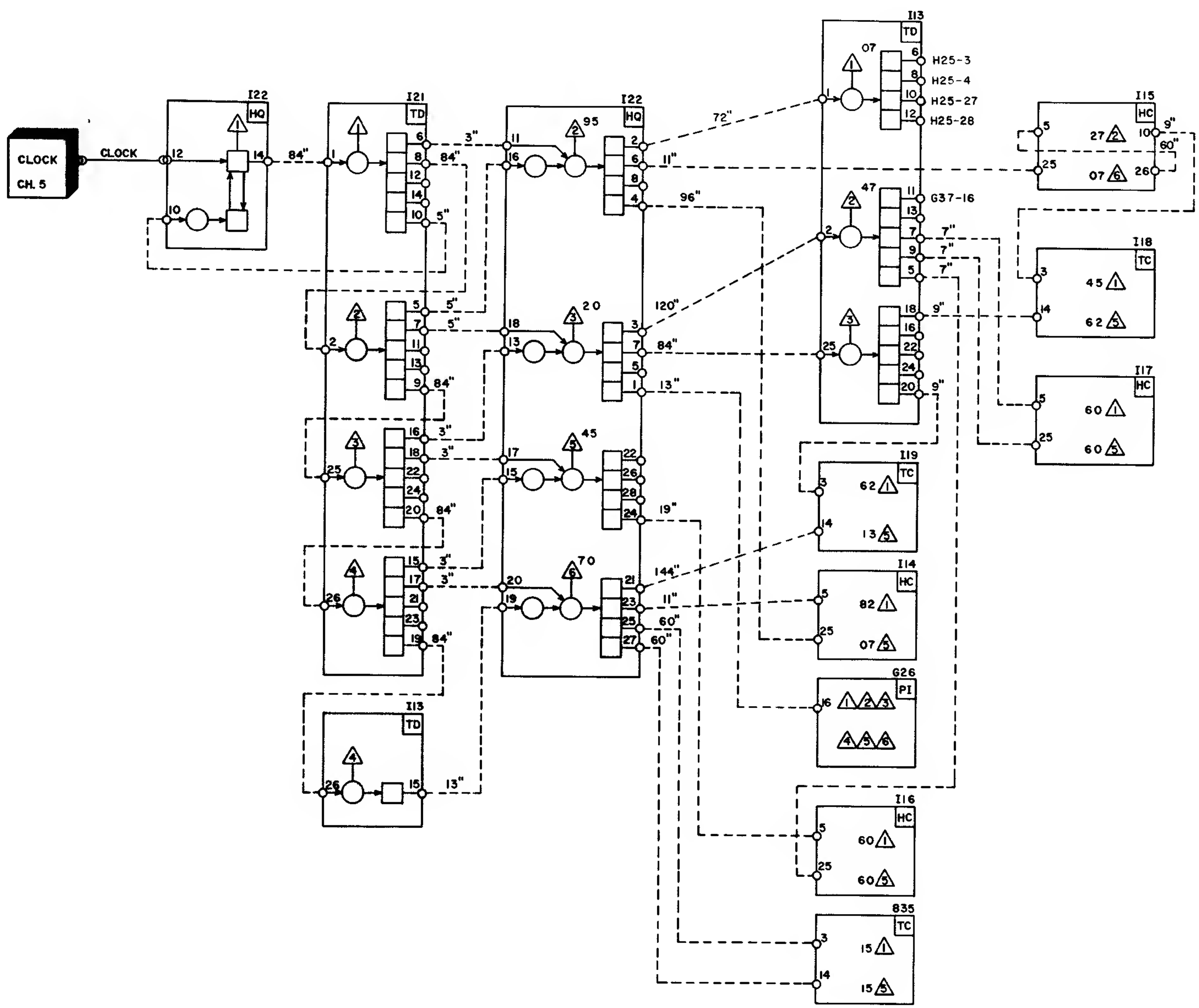
NOTES:

1. ADJUST LENGTH TO 25 NSEC BETWEEN LEADING EDGES OF PULSES ON SUCCEEDING TIP'S.
2. ADJUST LENGTH TO GIVE WIDTH OF 25 NSEC TO PULSE ON TIP'S.
3. SYNC TAKEN AT I22 TP2
4. REFERENCE TIME AT I22 TP3.

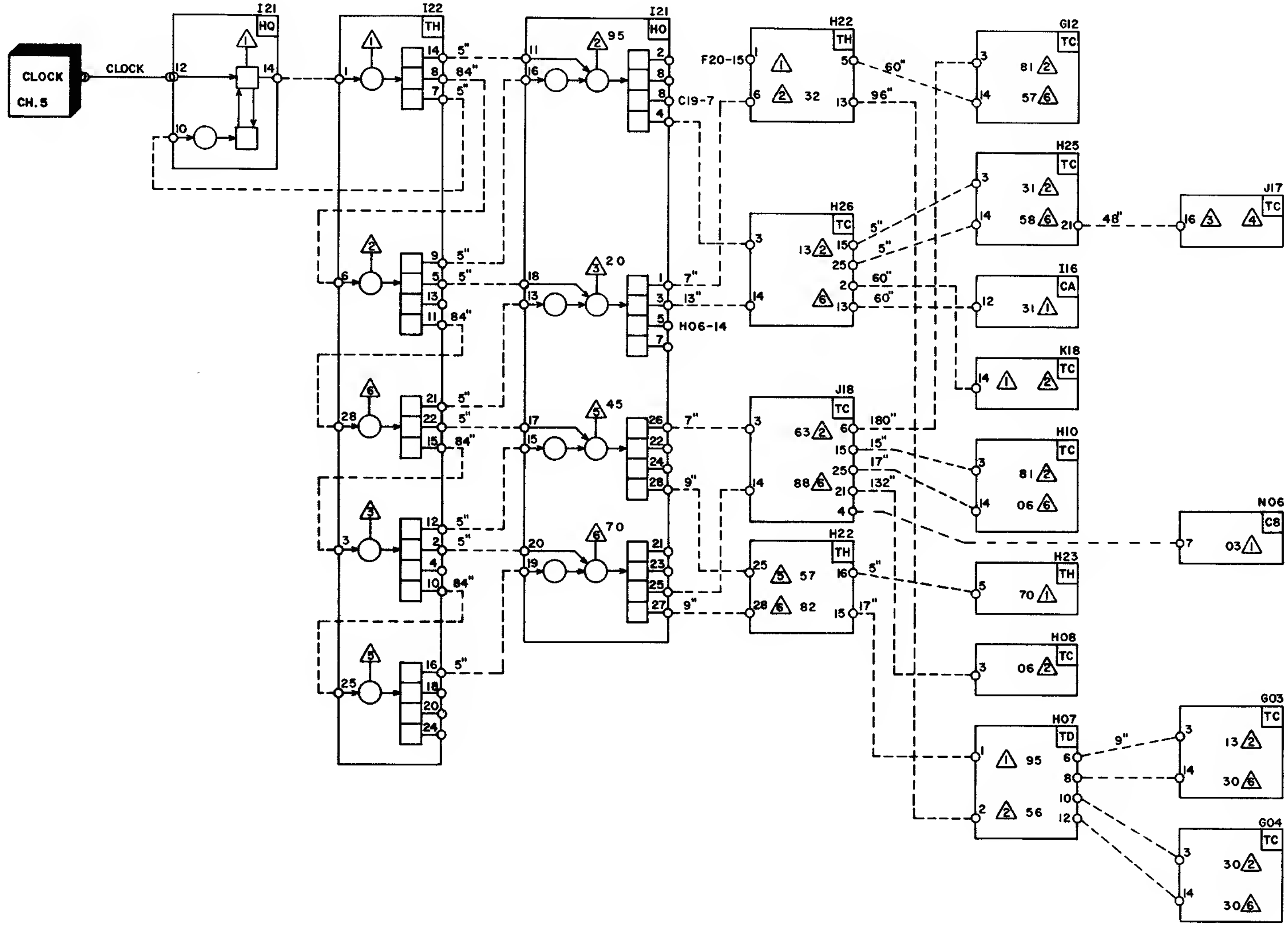
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH. 5 SERIALS 32 AND UP ONLY	PRODUCT 6601/04/13/14 SIZE C DRAWING NO 60119300 REV BT SHEET 273 12.3



CONTROL DATA CORPORATION	TITLE	PRODUCT
COMPUTER DIVISION	CENTRAL PROCESSOR CLOCK CH. 6	6601/04 SIZE: C DRAWING NO.: 60119300 REV: BT SHEET: 121 PAGE: 13



CONTROL DATA CORPORATION	TITLE CENTRAL PROCESSOR	PRODUCT 6601/04	
	CLOCK	SIZE C	DRAWING NO. 60119300	REV BT
COMPUTER DIVISION	CH. 7	SHEET 122	15



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH. 8	PRODUCT 6601/04/13/14 SIZE C · DRAWING NO. 60119300 · REV BT SHEET 123 · 17

ECS COUPLER CONTENTS

MODULE LOCATION INDEX

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ROW H	MODULE TYPE	PAGE
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07	PJ	7,
08	PJ	7,
09	PJ	7,
10	TR	13, 23, 25, 31
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10	PJ	13
11	MD	21
12	TH	19, 21, 31
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14	UM	15
15	TL	11, 21, 23
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17	WE	19
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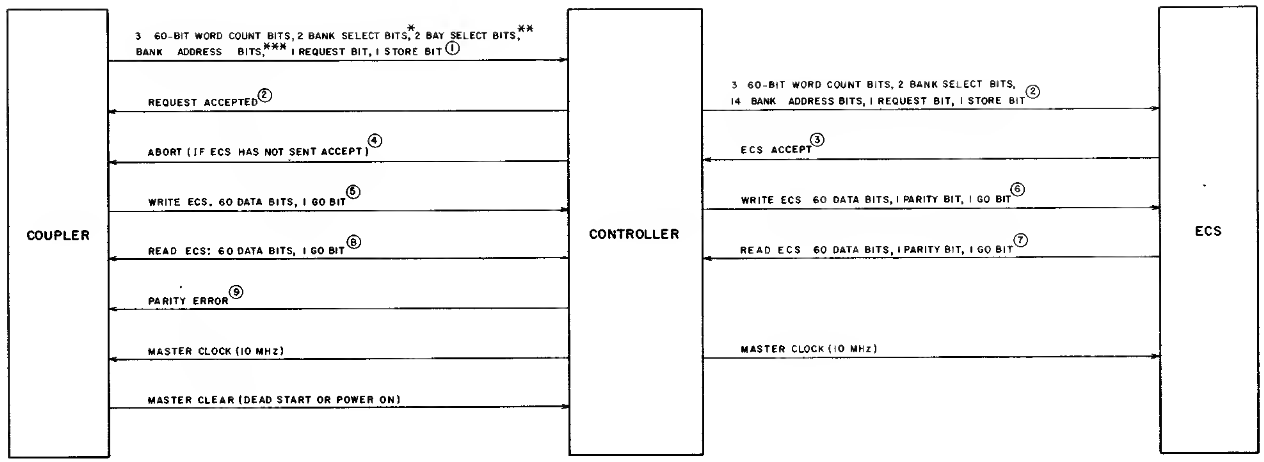


GENERAL DESCRIPTION

The ECS Coupler allows the CPU to communicate with ECS via the Controller. The coupler has two major functions. First, it computes the actual starting addresses in CM and ECS and checks to see if these addresses are out of range. This is the only error check made by the coupler. Second, it keeps count of the number of words transferred and terminates the transfer accordingly.

Most of the coupler's complexity arises from the fact that the programmer specifies initial addresses in CM and ECS and the number of 60-bit words to be transferred. However, ECS uses 8-word records and the coupler must automatically keep requesting new locations in ECS every eight words.

Coupler action can be interrupted by a PPU requesting CM. Action is started once the PPU read/write request is completed. Coupler action can also be interrupted if another computer is using ECS and the controller.

Coupler action is stopped if an Exchange Jump occurs. The transfer must be restarted at its beginning as intermediate values of word counts and addresses are not stored.

The coupler acts on an Abort or a Parity Error signal but relays them to CPU.

LOGICAL ELEMENTS

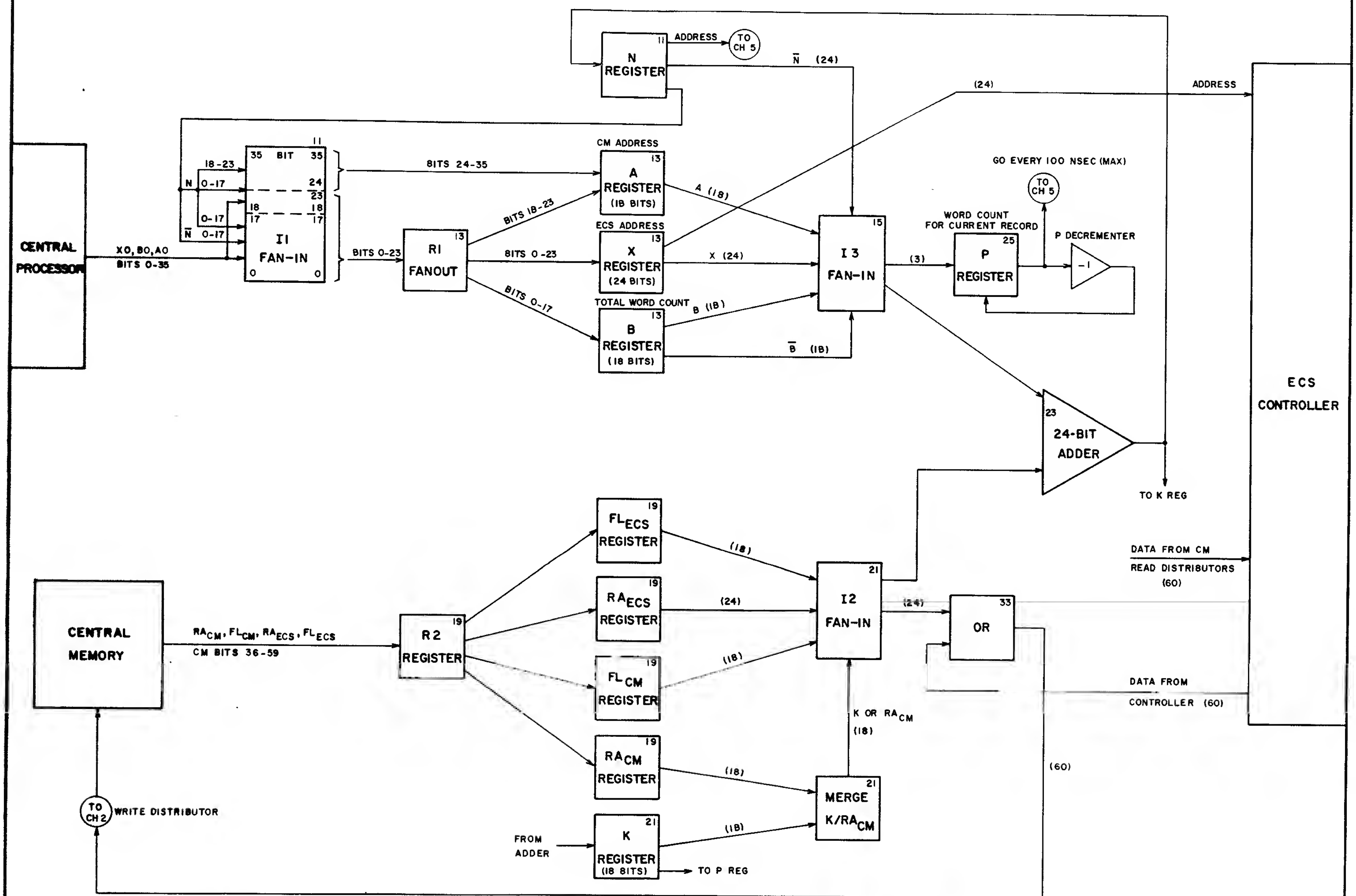
Four registers hold the values of Field Length for CM and ECS and the values of the Reference Address for CM and ECS. These values are not changed during a data transfer, and are restored, via the data paths, on an Exchange Jump.

The N and K registers are used for holding intermediate values generated during a transfer.

The adder is a 24-bit adder resembling 2 stages of the CPU Long Add unit.

P Register holds the 3-bit word count of the record in transfer. Its contents are decremented during a transfer.

The X, A and B Registers initially hold the same values as X_0, A_0 and B_0 respectively. X holds the ECS address and is incremented during a transfer; A holds the CM address and B the number of words left to transfer.



KEY: (60) = BANDWIDTH

33 ← THIS LOGIC IS SHOWN ON PAGE 33

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
ECS COUPLER
BLOCK DIAGRAM

PRODUCT
ECS COUPLER

SIZE	DRAWING NO	REV
C	60119300	B

SHEET 278 PAGE 1

SEQUENCE OF OPERATIONS

INTRODUCTION

Coupler operation is divided into three parts:

1) Transfer Setup.
This portion is performed only at the beginning of a transfer and is not repeated.

2) Record Setup.
This part of the operation is performed before each record transferred.

3) Data Transfers.
If 524K of ECS are used, the data can be transferred at the rate of one word every 100 nsec. The coupler handles 8-word records and to sustain this rate, it must request a new record while the data transfer is in progress. That is, the Record Set-Up for the next record is performed at the same time as the data transfer. (See block transfers below.)

Exceptions to the above occur when error conditions arise or a PPU wishes to read or write in memory. This is discussed on the pages where this logic is shown.

TRANSFER SETUP

On any Exchange Jump, FL(ECS), FL(CM), RA(ECS), RA(CM) are sent from the package to the coupler.

When an ECS instruction is translated,
1) The timing chain is started.
2) The contents of X0 and A0 are sent to the coupler X and A registers (These address relocation quantities must be stored prior to instruction execution.)
3) The Clear signal on B0 is dropped and the word count (Bj + K) is formed in the increment unit and sent to B0 which is sent in turn to the coupler B register.

All required values are now stored in the coupler. Note that the values of FL(ECS), FL(CM), RA(ECS) and RA(CM) are not changed during on ECS transfer. They are restored to CM if an Exchange Jump occurs.

4) The coupler then checks to see if the initial addresses are in bounds. If either CM or ECS Field Length errors occur, the transfer is terminated.
5) The first ECS address is computed, (X+RA(ECS)), and stored in X. This absolute address will be updated after each record.

RECORD SETUP

FIRST RECORD

ECS reads/writes eight 60-bit words at once. This single record is disassembled/assembled in ECS under control of the lowest 3 bits of the ECS address (see Definition Of Word Count Bits on diagram). These bits specify where in the record the operation should start. ECS always continues from the starting point to the end of record. If only word three is required, then the record at that address sends five words starting at word three. However, the word count is one, and this is entered in the P register. The single word is accepted and the transfer concluded even though ECS sends the remaining four words.

First record proceeds as follows:
1) The first record may be a partial record. Therefore, the lower 3 bits of X (60-bit word count bits) are subtracted from 10_8 to give the number of words to be transferred in this record. This result is sent to K.
2) K is checked against B. If K-B is negative, more than one record is to be transferred. K is sent to P as this number of words is the first record. (If K-B is positive, then this becomes the last record and B is sent to P (see Last Record).
3) B is reduced by K words.
4) The ECS address, Store bit and Request bit are sent to the controller.
5) The ECS address is incremented by K. This means that the lower 3 bits of X are clear and that the following records must be complete ones.
6) The Accept is received from the controller. The coupler waits until this occurs.
7) The Central Memory address, (A+RA(CM)), is computed and stored in the A register. It is also sent to the Exchange Address Counter (EAK), where it is incremented by the P decrementer Go pulses.
8) The P decrementer is enabled and the data transfer is started.

SECOND RECORD

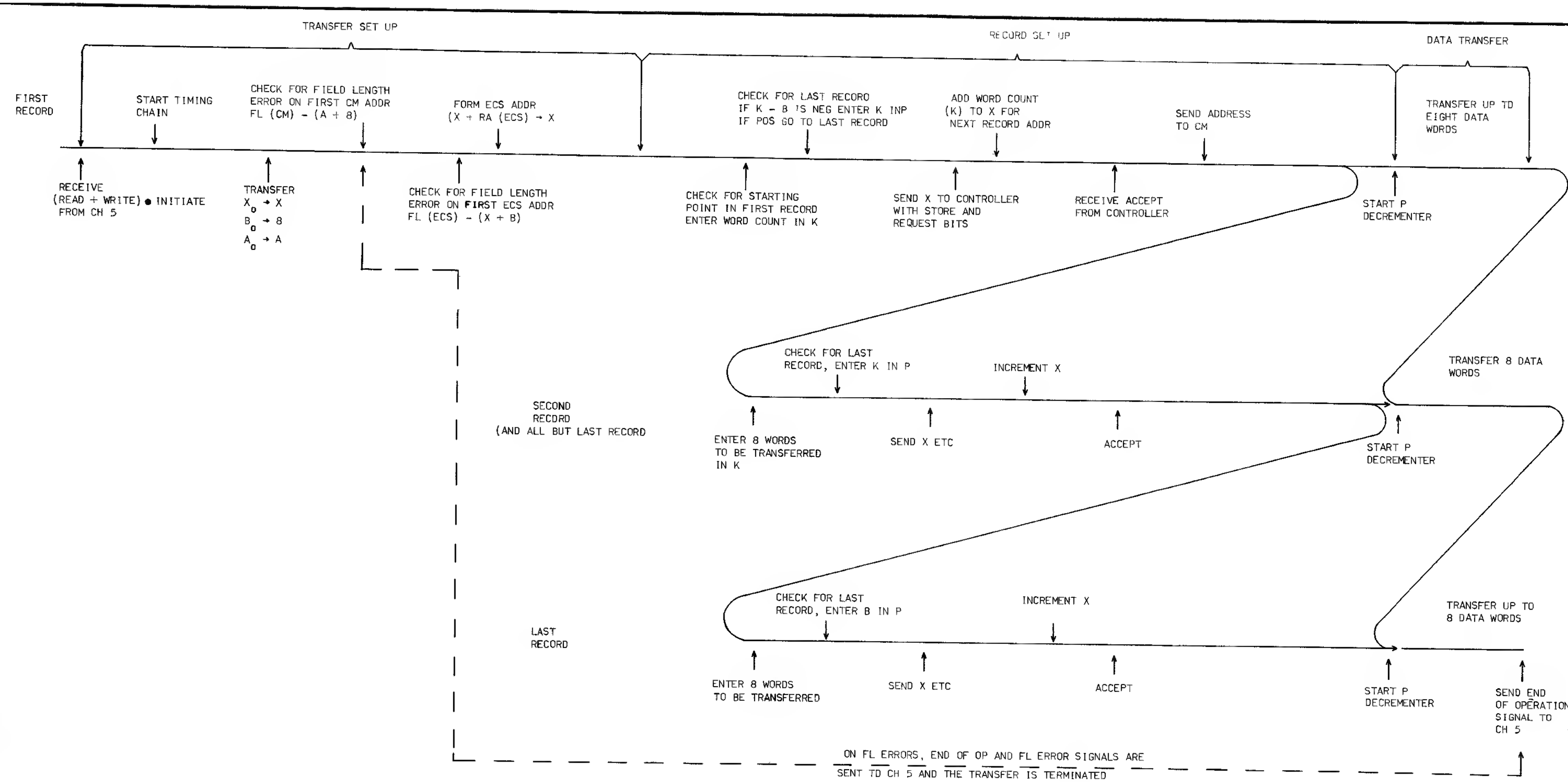
While the data is being transferred for the first record, the second Record Setup is starting the next ECS bank into its Read/Write cycle. The differences between the second record (or any intermediate record) and the first are:
1) Since they cannot be partial records, step 1) simply transfers 10_8 to K. Also the ECS address is incremented by 10_8.
2) Since the Exchange Address counter holds the CM address, a new address is not sent to CPU as in 7.

LAST RECORD

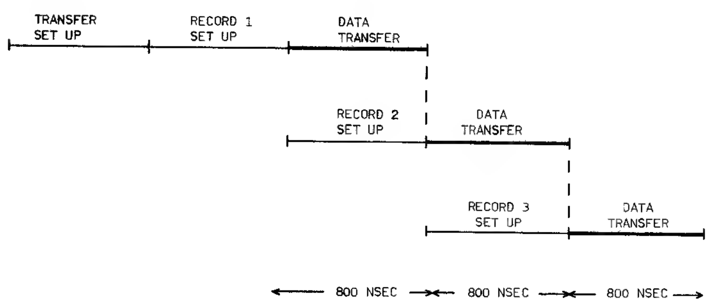
Any record may become a last record if the K-B test is positive. If so, B is sent to P register. Since B may be 0-7, the record can be a partial record but only in that it is terminated early (when B is less than 7). Note that a Last Record is different only in that the parameters for the record following are not generated and that an End Of Operation signal is sent to CPU.

DATA TRANSFERS

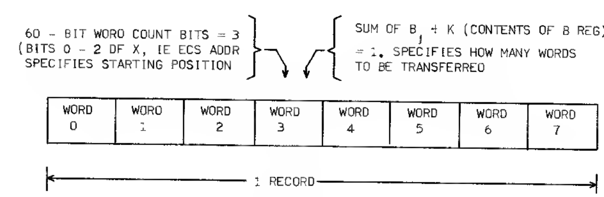
Note that data transfers must be continuous; that is, non-consecutive addresses are not possible in a block transfer. However, it is possible to reference a single word in ECS.



SEQUENCE OF OPERATIONS



BLOCK TRANSFERS



DEFINITION OF WORD COUNT BITS

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE SEQUENCE OF OPERATION	PRODUCT ECS COUPLER		
		SIZE C	DRAWING NO. 60119300	REV. BL
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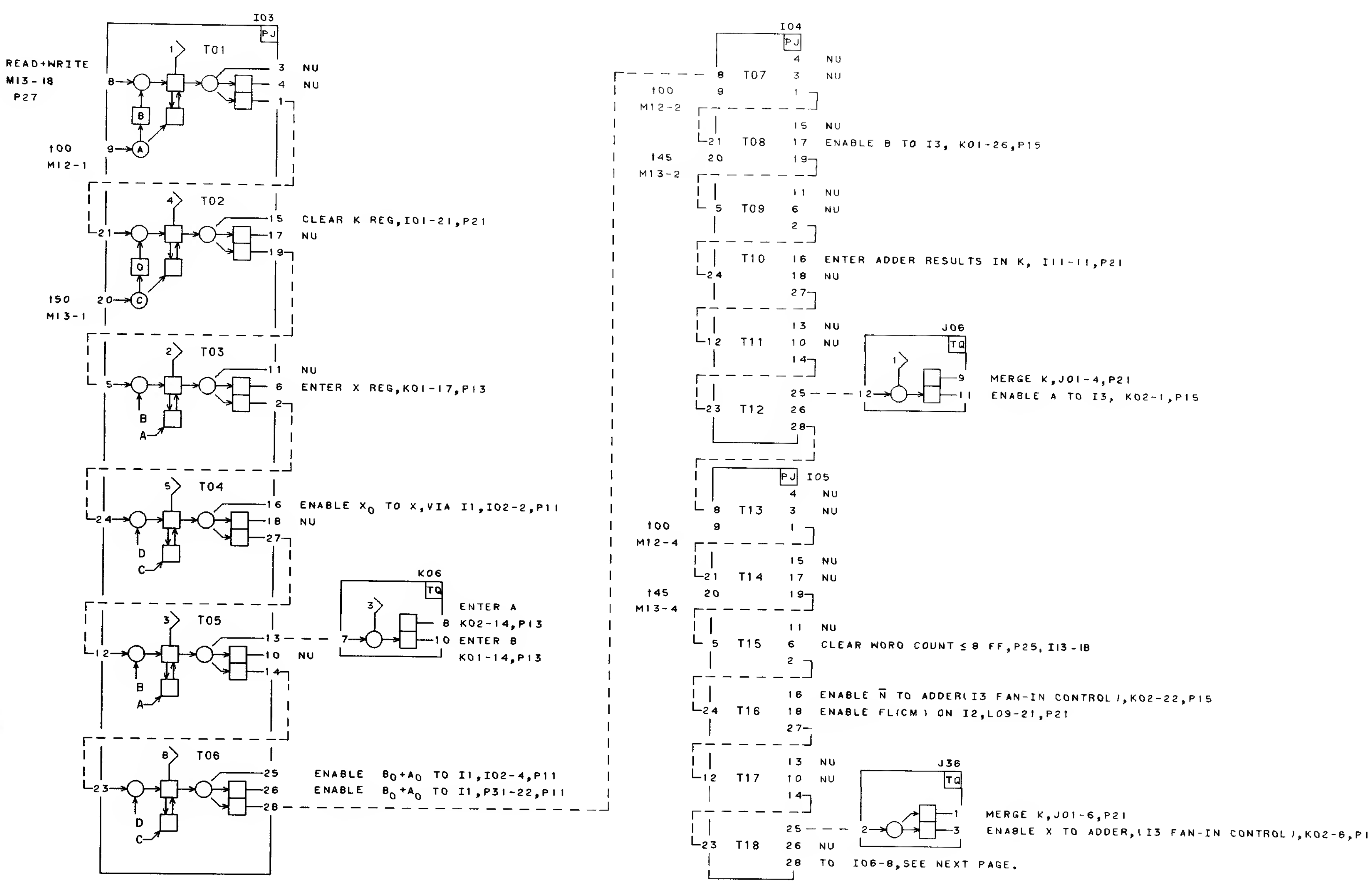
TIMING CHAIN DESCRIPTION

Each FF in the timing chain is set for 100 nsec, but there is only a 50 nsec delay between the setting of consecutive FFs. The timing chain runs for 2.4 usec minimum and controls most of the coupler's operations. Part of the timing chain (T01 to T18) is used only in Transfer Setup. Note that all adder results go unconditionally to N, which is cleared every 100 nsec.

TRANSFER SETUP

The Initiate, Read (or Write) FFs are set. Read/Write FF is set. Timing chain is started at t00.

T02	Clear K register
T03 } T04	Enter X_0 register into X via I1.
T05 } T06	Enter A_0 and B_0 registers into A and B via I1.
T08 } T10	Send B (Word Count) to I3, and to adder. Adder results to K. This is a transmission of B to K in preparation for FL checks.
T12	A and K to adder; result to N register.
T16	Perform FL check, (FL(CM) - (A+B)), by sending $\overline{N}$, (A+K), and FL(CM) to adder; results to N. If error, send signal at T20.
T18	X and K to adder, result to N register.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE TIMING CHAIN T01-T18	PRODUCT ECS COUPLER	
		SIZE C DRAWING NO 60119300	REV
		SHEET 280	PAGE 5

T20 Send Error Signal (T16); that is, N register is negative. (Bit 23 set)

T21 Clear K Reg.

T22 Perform FL check (FL(ECS) - (X+B)) by sending N, X+B, and +FL(ECS) to adder; results to N register. If error, send signal at T25.

T23 Set First FF.

T24 Perform X+RA(ECS); result to N register.

T25 Send Error Signal (T22). That is, N register is negative.

T26 For first record only, A and RA (CM) and sent to the adder.

END TRANSFER SETUP

START RECORD SETUP

If this was an intermediate record, the Record Setup would now begin for the next record. If the record in progress was the last record, the Read 2 or Write 2 FFs would have been cleared and the timing chain would not be restarted.

T27} T28} Enter X with absolute ECS address from N (first record only).

T28 Set bit 3 of K; mask all bits of I3 Fan-In (extend sign) except 0-2. Send K and N to adder. X and N both contain the actual ECS address. Since the lower 3 bits of X may not be zero (partial record) the coupler must determine what to enter in P. This is only true on the first record.

from N we have:	7 ⟵ 7X	(note that the 7's are masks and the X is the complement of the 60-bit Word Count)
from K we have:	0 ⟵ 010	
Results from adder: (entered in K)	0 ⟵ 0X+1	(end around carry)

T29 Clear K. Enter A (if this record is not the first) with A+10_8 (see T42). If this is the first record, send $\overline{N}$ to A. That is, enter the CM address in A (see T26)

T30 Enter adder results in K (T28). This is the number of words to be transferred for this record. Send ECS address, Request, and Store Bit to the Controller. The check will now be made to determine if this is last record and if so, how many words will be transferred. This is done by subtracting the Word Count (Bj + K), now in B, from K.

T32 $\overline{B}$ and K to adder; extend upper bits (18-23) of adder input to make B negative.

T34 K and X to adder. This is updating the ECS address by the word count. Note that for the first pass this made any address have its lower 3 bits all zeroes. Thereafter, any record will be started at word 0. Also, if this is any record other than the first, it amounts to adding 10_8 to X, which in turn implies incrementing the address of the record in ECS by 1.

T35 Enter N in B register. This is the result of K-B complemented, which is B reduced by K. If N is negative, B was larger than K and this is not last record and K is entered in P at T37. If it is positive, the Word Count ≤ 8 FF is set and B is entered in P at T39.

T37 K to P if not last record. Send N to X. This is the result of the K and X addition at T34 and is the ECS address for the next but one record. The setting of T38 is dependent upon an Accept being received from the Controller. Coupler action, therefore, waits until this is received. If the Accept is not received, but an Abort is, then the timing chain proceeds. If the record in transfer is the last record, (that is, if the Read Last Record FF is set) this FF blocks the timing chain and prevents the requesting of any further records.

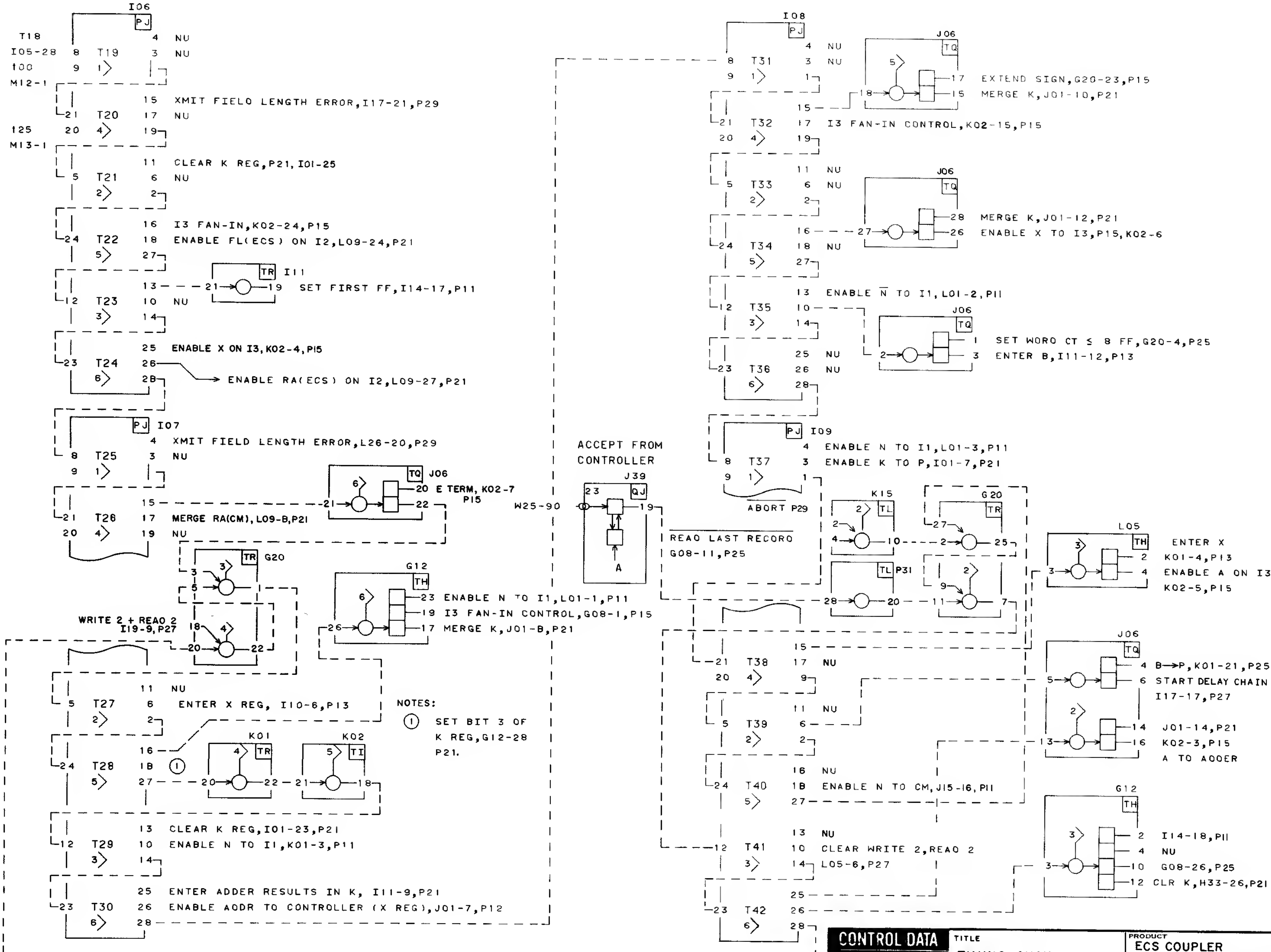
T38 Send A through the adder and enter in N. N will send A to CM (see T40). Enter X with N (see T37).

T39 Send B to P if last record. Start delay chain if this is a read operation; this is to delay the start of the decrementer long enough to get the data back from ECS.

T40 Send N to CM. This is the result of the A+RA(CM) computation and occurs on the first record only.

T41 Clear Write 2 and Read 2 FF if this is last record. Enable decrementer.

T42 Send A and K to adder. This updates the CM address by 10_8. This new address is entered in A at T29. It is not sent to CM each record but is available if needed; that is, after a PPU interrupts the transfer. Clear First FF and set Read Last Record FF if Word Count ≤ 8 is set. Set T27FF which implies starting a new Record Setup sequence. Note that T27FF is set 25 nsec after T42 and T28FF is set 75 nsec after T42. Therefore, T42 at t75 is the same time as T28 at t00. This overlap ensures that K=10_8 and A are sent to the adder at the same time.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: TIMING CHAIN T19 - T42

PRODUCT: ECS COUPLER

SIZE: C | DRAWING NO: 60119300 | REV: AL

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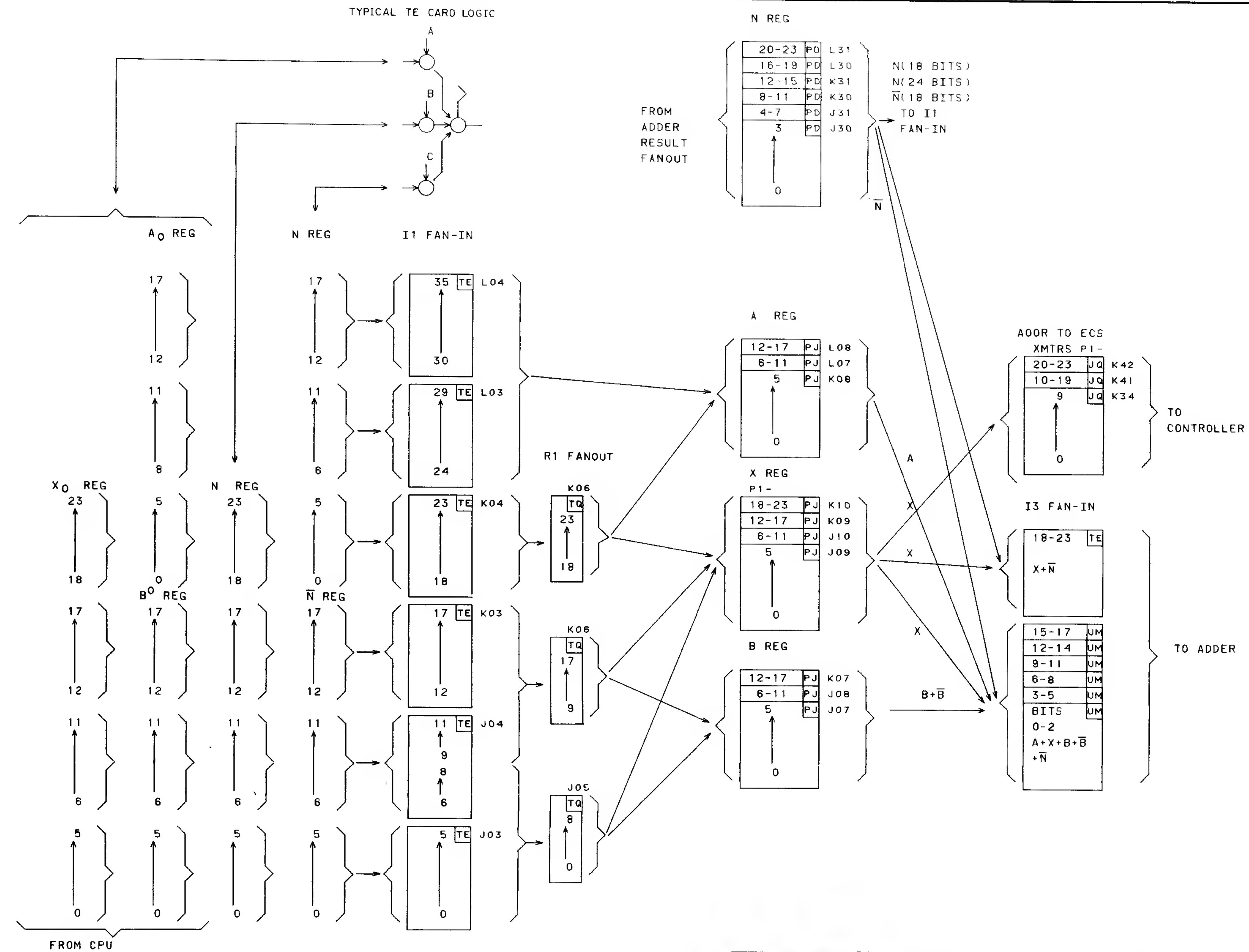


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE DATA FLOW I I1 AND I3 FAN-INS R1 FANOUTS X,A,B, AND N REGS	PRODUCT ECS COUPLER SIZE C · DRAWING NO 60119300 · REV R1 SHEET 282 · PAGE 9

N REGISTER

This is a 24-bit register which can send its contents to:

1) the adder via I3 fan in.
2) X, A, and B registers via I1 fan in.
3) the Peripheral Address Network; that is, to CM through the same path as a PPU Address. This is only done after A+RA (CM) is computed.

The results of all adder operations are unconditionally entered in N. However, these results are then lost after 100 nsec because of the clear/set input.

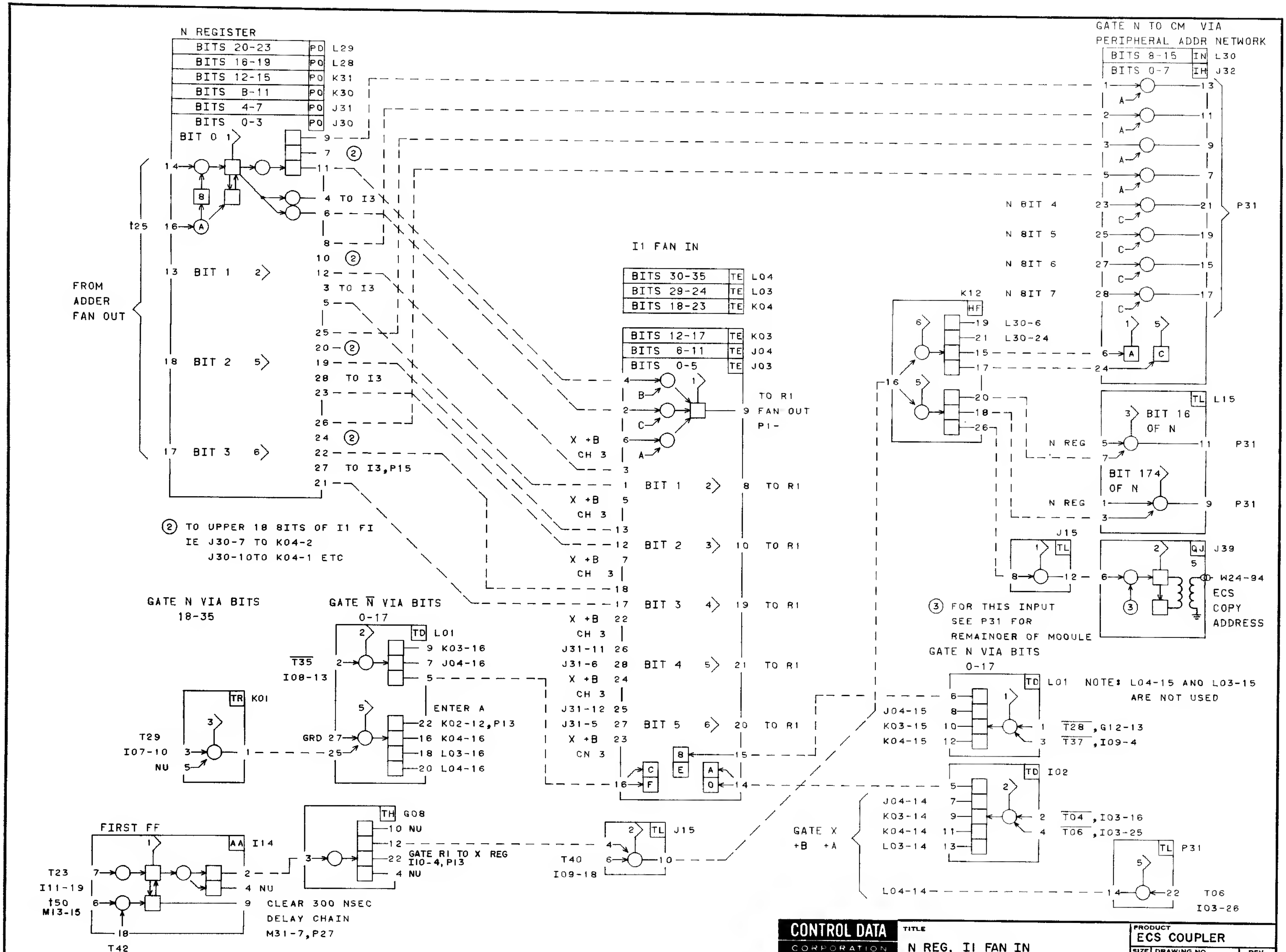
The uppermost bit of N is used to check for negative results from the adder. This is done in the Field Length tests and the K-B tests.

I1FAN IN

This directs addresses from N (or $\overline{N}$) or from Chassis 3 Read Distributor. When the timing chain is started, the contents of X_0, B_0 and A_0 are entered in the couplers X, B and A registers via the I1 fan in. Once this has been done, only the contents of N (or N) are sent through I1.

FIRST FLIP FLOP

This FF is used to control addresses that are required for the Transfer Setup and the First Record Setup. Once cleared (at T42) it is never set again during a block transfer. Therefore, the initial address in CM is sent only once and is incremented in the EAK (in the CPU), by signals from the P decrementer. An exception to this occurs if the transfer is interrupted by a PPU Read/Write. In this case a new CM address is required. The ECS Copy Address signal is used to enter CM address in the Exchange Address Counter.



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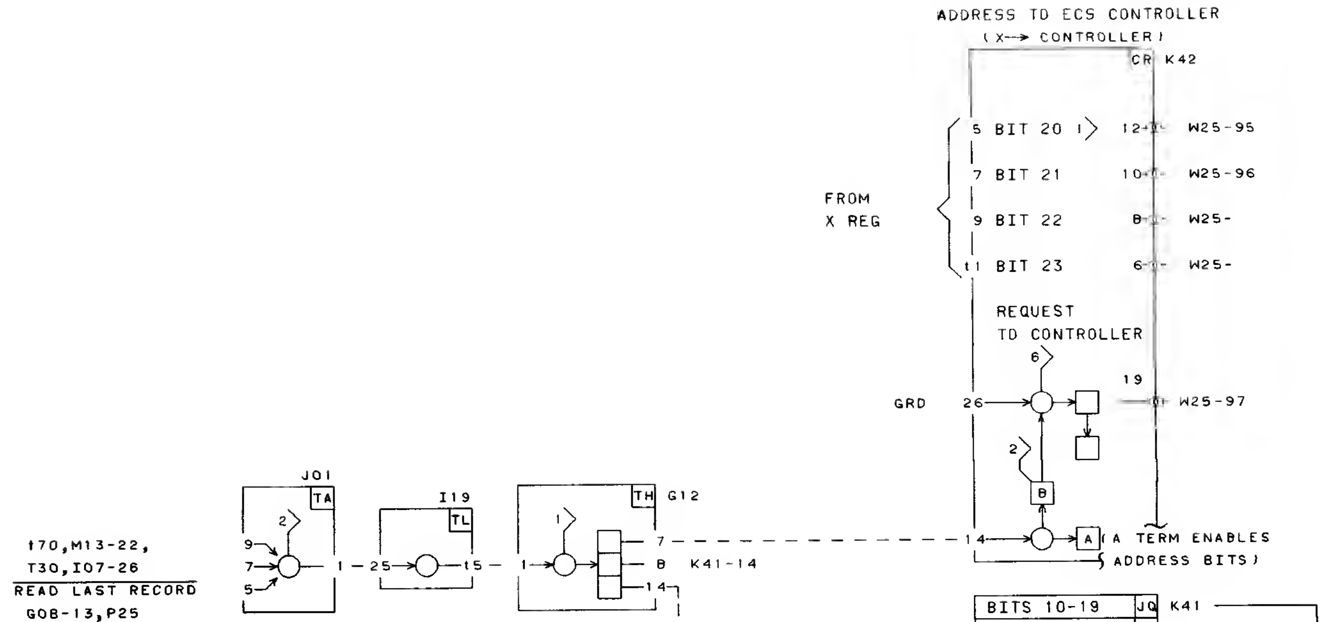
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

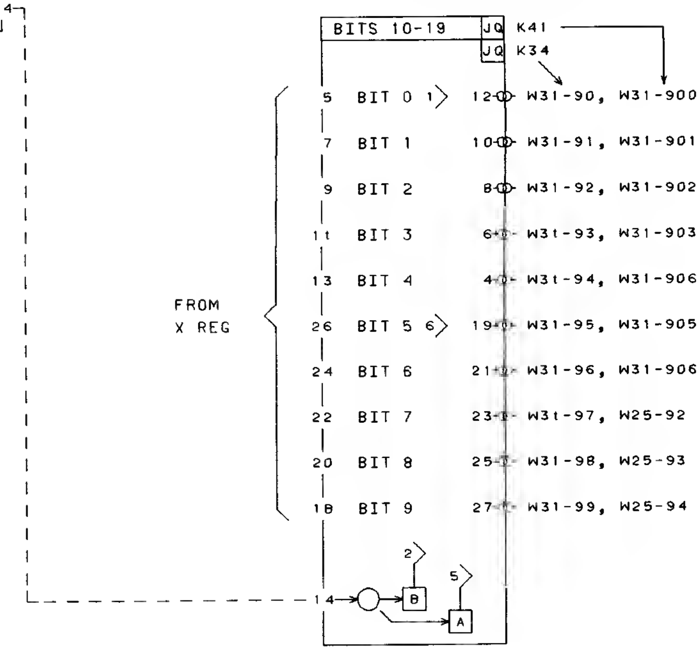
TITLE: N REG, I1 FAN IN FIRST FF

PRODUCT: ECS COUPLER

SIZE: C DRAWING NO: 60119300 REV: B1

SHEET: 283 PAGE: 11





A, B AND X REGISTERS DESCRIPTION

A REGISTER

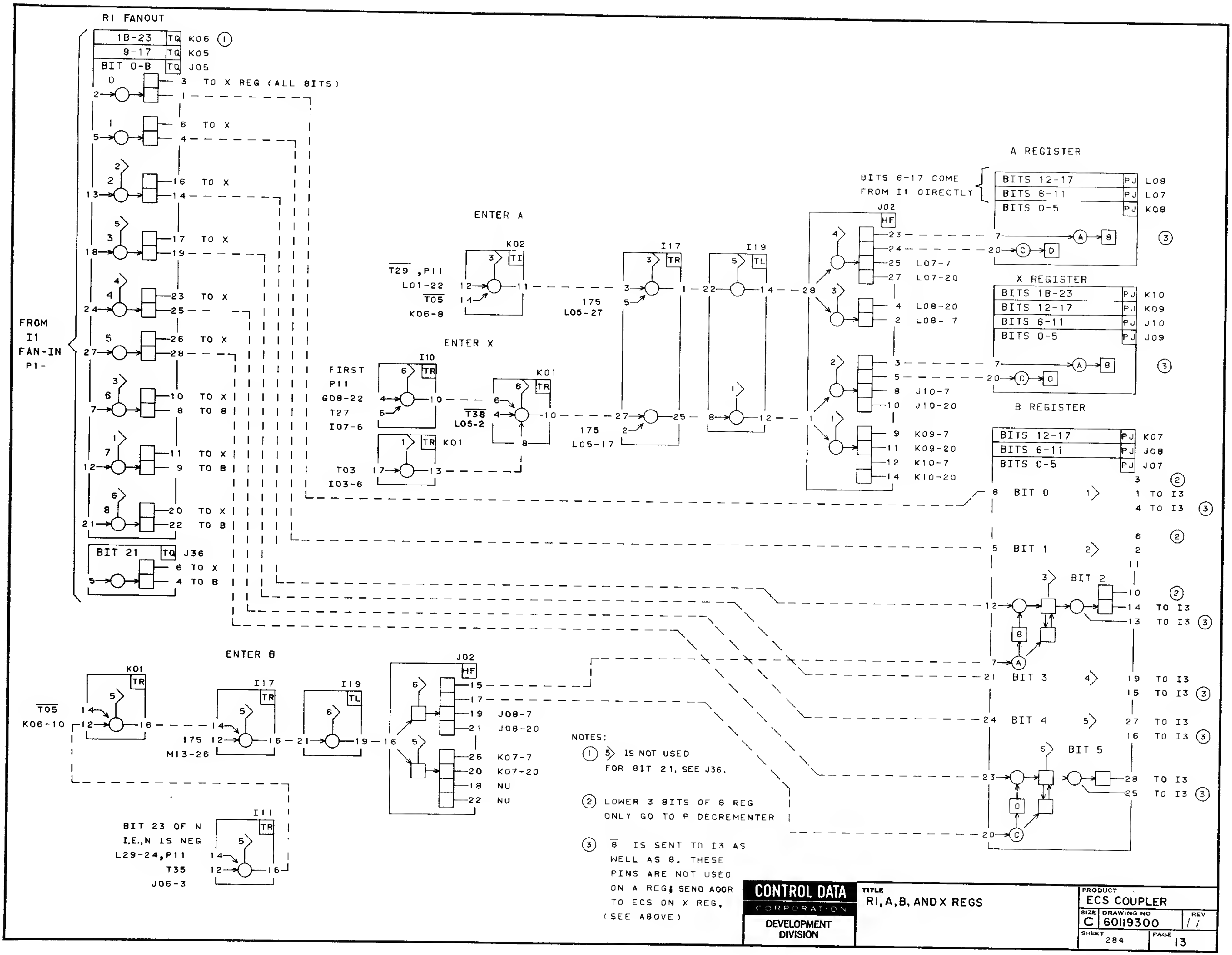
This is an 18-bit register which initially holds the contents of A_0 (relocation quantity for CM addresses). During Transfer Setup, RA(CM) is added to A and the result is entered in A and sent to the FAK. The initial CM address (page 11) A is updated every eighth word (once every record) by a count of 8; however, this updated address is not sent to CM for each record.

B REGISTER

This 18-bit register holds the total number of words to be transferred. Initially, it has the contents of B_0 (Bj + K), but it is decremented by the number of words to be transferred in the next record. This is done during Record Setup. If it is the last record, the lower 3 bits of B are sent to the decrementer. This condition is determined by N being positive, that is, K was greater or equal to B. B is not changed if this condition is met.

X REGISTER

This 24-Bit register holds the ECS address. It is updated by 10_8 for each record request made to the ECS Controller. The initial contents of X is the relocation quantity X_0. During transfer set up time RA(ECS) is added to X and the result entered in X. The address is sent to the controller at T30, but the updating for the address took place during the previous Record Setup time. This is done to ensure sufficient time for the Request to be processed by the Controller. Note that the Store Bit transmitter is on module K42 and is sent at the same time, (see page 27).


RI FANOUT
18-23 TQ K06 1
9-17 TQ K05
BIT 0-8 TQ J05
TO X REG (ALL BITS)
TO X
TO B
BIT 21 TQ J36
FROM I1 FAN-IN P1-
ENTER A
K02 TI
T29, P11
L01-22
T05
K06-8
175 L05-27
I17 TR
I19 TL
J02 HF
L07-7
L07-20
L08-20
L08-7
J10-7
J10-20
K09-7
K09-20
K10-7
K10-20
ENTER X
I10 TR
FIRST P11
G08-22
T27
I07-6
K01 TR
T38 L05-2
175 L05-17
T03 I03-6
A REGISTER
BITS 6-17 COME FROM I1 DIRECTLY
BITS 12-17 PJ L08
BITS 6-11 PJ L07
BITS 0-5 PJ K08
X REGISTER
BITS 18-23 PJ K10
BITS 12-17 PJ K09
BITS 6-11 PJ J10
BITS 0-5 PJ J09
B REGISTER
BITS 12-17 PJ K07
BITS 6-11 PJ J08
BITS 0-5 PJ J07
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
TO I3
ENTER B
K01 TR
T05 K06-10
175 M13-26
I17 TR
I19 TL
J02 HF
J08-7
J08-20
K07-7
K07-20
NU
BIT 23 OF N
I.E., N IS NEG
L29-24, P11
T35
J06-3
I11 TR
NOTES:
1 5 IS NOT USED FOR BIT 21, SEE J36.
2 LOWER 3 BITS OF B REG ONLY GO TO P DECREMENTER
3 B IS SENT TO I3 AS WELL AS B. THESE PINS ARE NOT USED ON A REG; SEND ADDR TO ECS ON X REG. (SEE ABOVE)
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE RI, A, B, AND X REGS
PRODUCT ECS COUPLER
SIZE C
DRAWING NO 60119300
REV
SHEET 284
PAGE 13

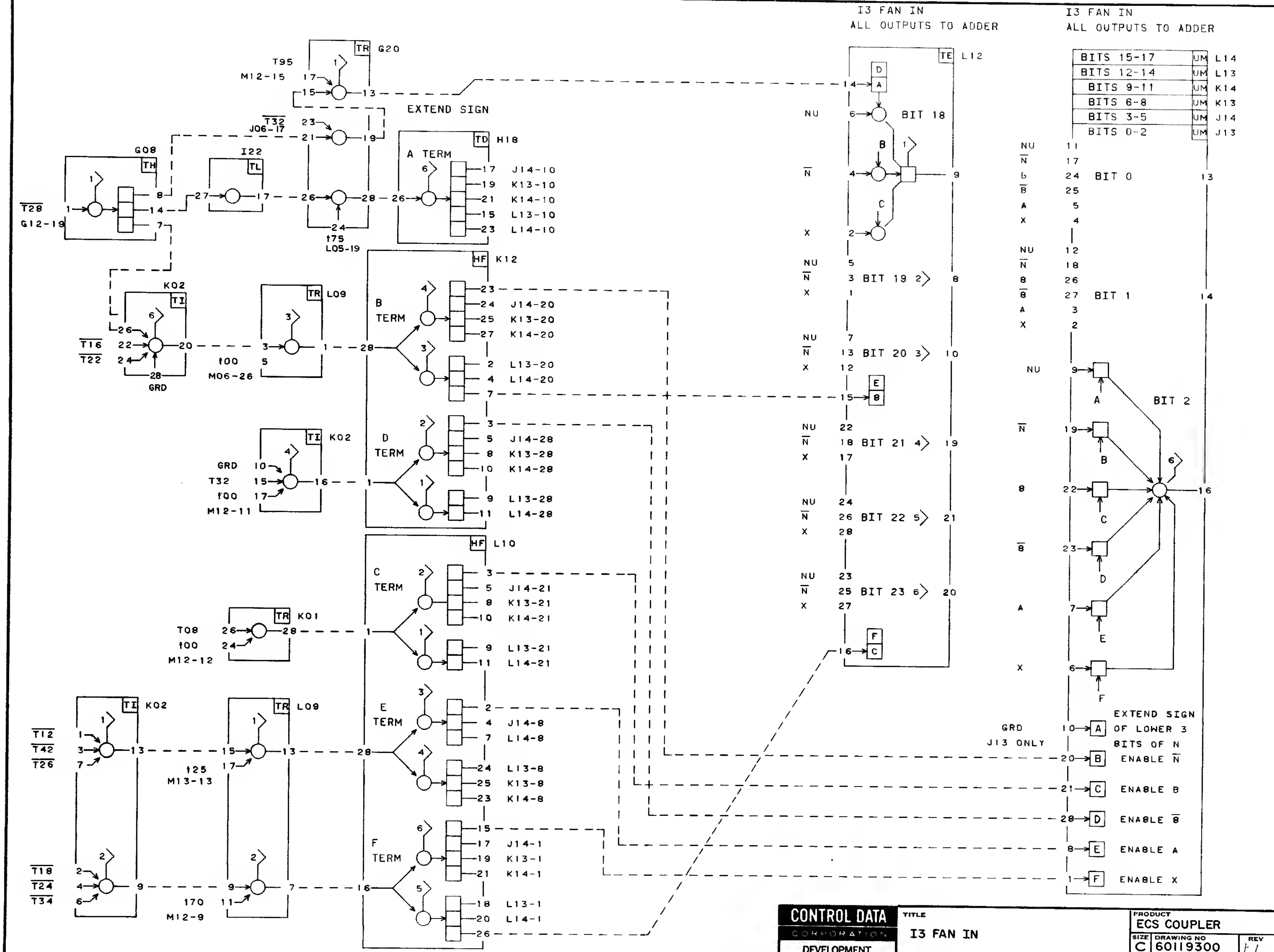
I3 FAN IN DESCRIPTION

The I3 Fan In allows the X, B, A or N registers to enter the adder.
Note:

1) The lowest 3 bits of the fan in are gated by the timing chain only.

2) Bits 3 through 23 can be forced to ones by the extend sign (A term). This is done at T28 to extend the negative sign of the complement of the lower 3 bits of X register. This is done when $\overline{N}$ (holding the newly updated ECS address) and K are sent to the adder when the coupler is determining the number of words to be transferred on the next record.

3) Bits 18 through 23 can be forced to ones by the extend sign (A term). This extends an 18-bit negative number to 23 bits. The sign is extended at T16 when (A+K) is in N and is to be subtracted from FL(CM) for Field Length checks. At T32 the K-B test is performed with B being sent to the adder, and its sign is therefore extended.



6697

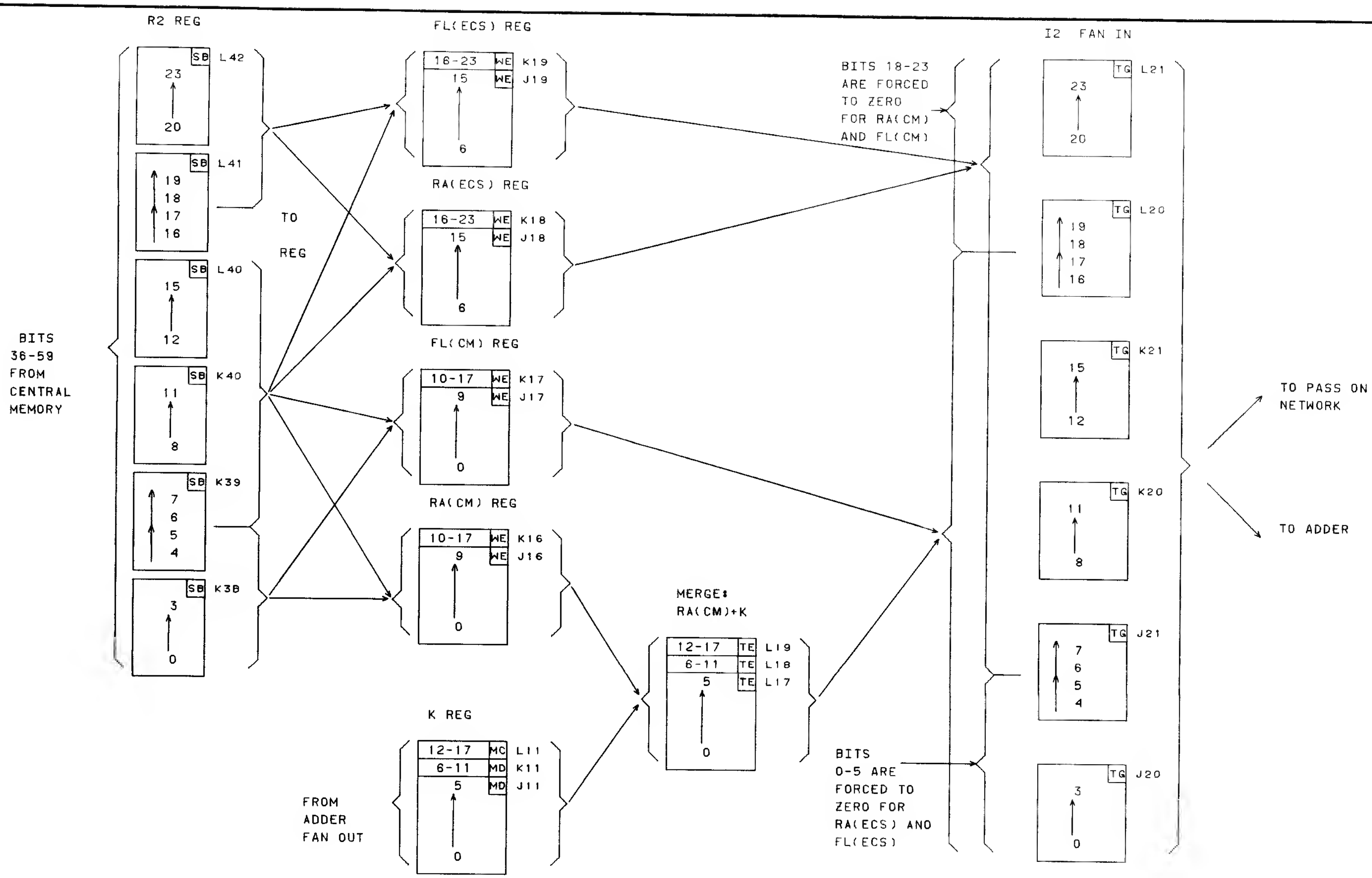
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE I3 FAN IN

PRODUCT ECS COUPLER

SIZE C DRAWING NO 60119300 REV

SHEET 285 PAGE 15



#6698

CONTROL DATA
CORPORATION
DEVELOPMENT DIVISION

TITLE
DATA FLOW 2
R2, FL AND RA REGS
I2 FAN-IN

PRODUCT
ECS COUPLER

SIZE	DRAWING NO	REV
C	60119300	

SHEET	PAGE
286	17

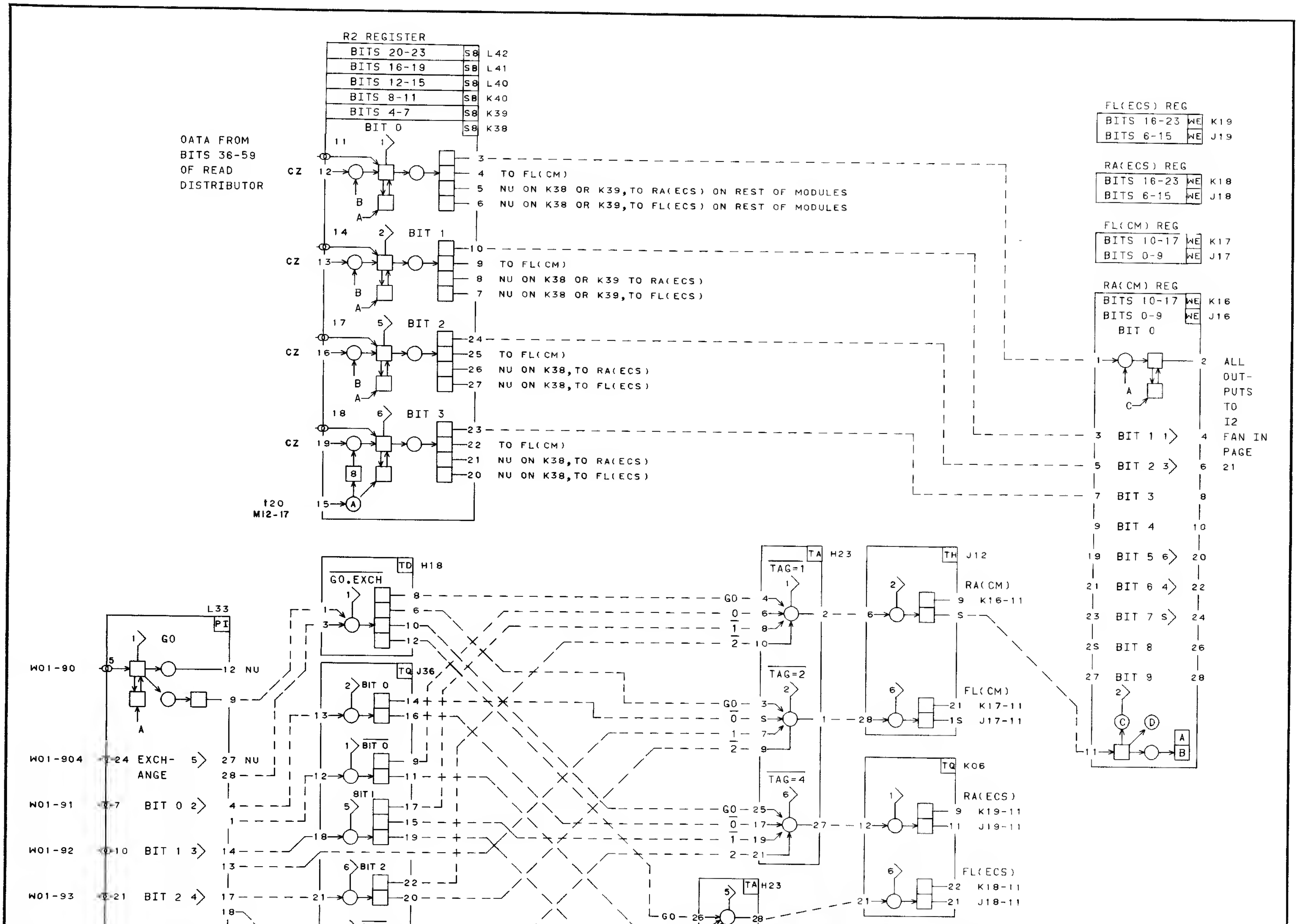
R2, RA AND FL REGISTERS

R2 REGISTER

This is a 24-bit catching register. Its contents are directed to the RA or FL registers by the address tags. These tag bits are the Increment Unit to A bits which are not used during ECS instructions and are therefore assigned to directing the ECS and CM parameters.

RA AND FL REGISTER

These hold the RA and FL quantities from the Exchange Jump package. Note that the lower 6 bits of the ECS registers do not exist.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE R2, FL(CM), FL(ECS), RA(CM) AND RA(ECS) REGISTERS

PRODUCT ECS COUPLER

SIZE C DRAWING NO 60119300 REV 11

SHEET 287 PAGE 19

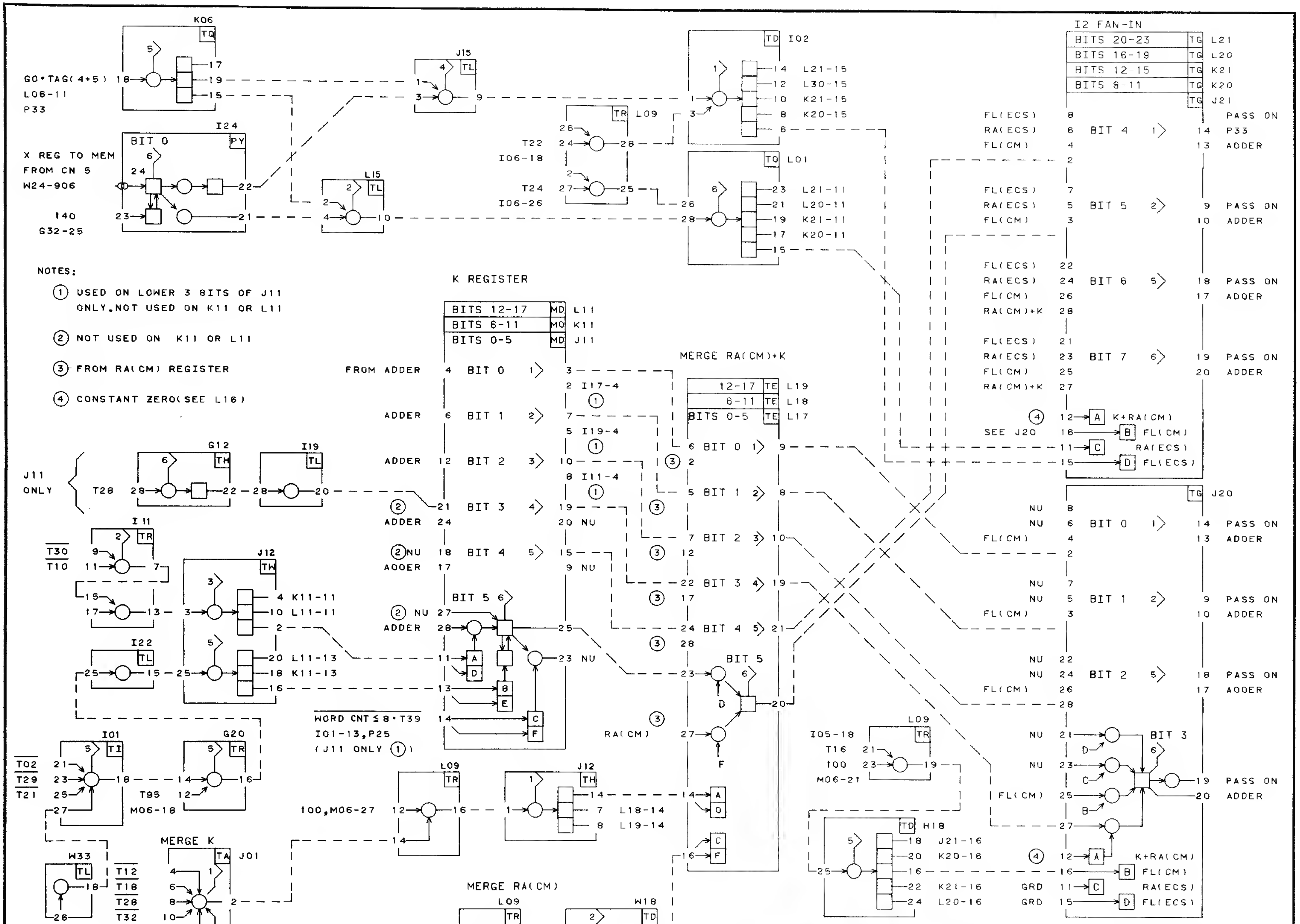
I2 FAN IN AND K REGISTER DESCRIPTION

K REGISTER

This 18-bit register holds the word count for one record. It also can have bit 3 forced to a one, which is used to increment quantities by 10_8. It sends its contents through the I2 fan out to the adder. Its inputs on I2 are shared with RA(CM) register and they are controlled by the merge RA(CM) or K gates which allow one or the other to I2. The lower 3 bits of K are sent to the P register except on the last record.

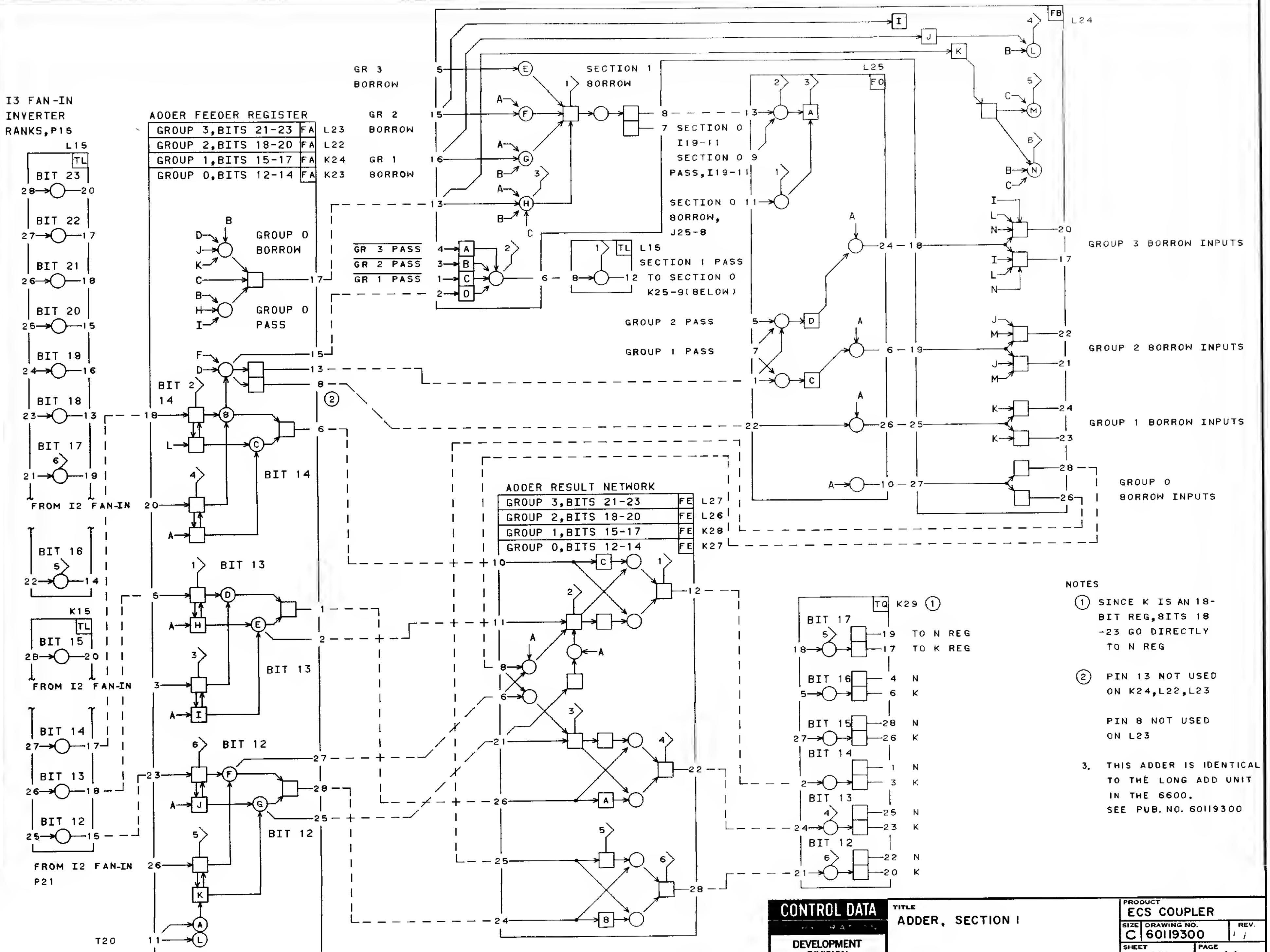
I2 FAN IN

This fan in allows RA, FL and K to send operands to the adder or to the pass on network. The latter would be done only if an Exchange Jump occurred. Since the lower 6 bits of the ECS registers do not exist, their inputs on I2 are not used. Also, since RA(CM) and K are controlled by the merge gates, their gating term (A) on I2 always a logical one output.



NOTES:
1. USED ON LOWER 3 BITS OF J11 ONLY, NOT USED ON K11 OR L11
2. NOT USED ON K11 OR L11
3. FROM RA(CM) REGISTER
4. CONSTANT ZERO (SEE L16)

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: I2 FAN-IN, MERGE RA(CM) REG, & K REG	PRODUCT: ECS COUPLER
		SIZE: C DRAWING NO: 60119300 REV
		SHEET: 288 PAGE: 21



NOTES

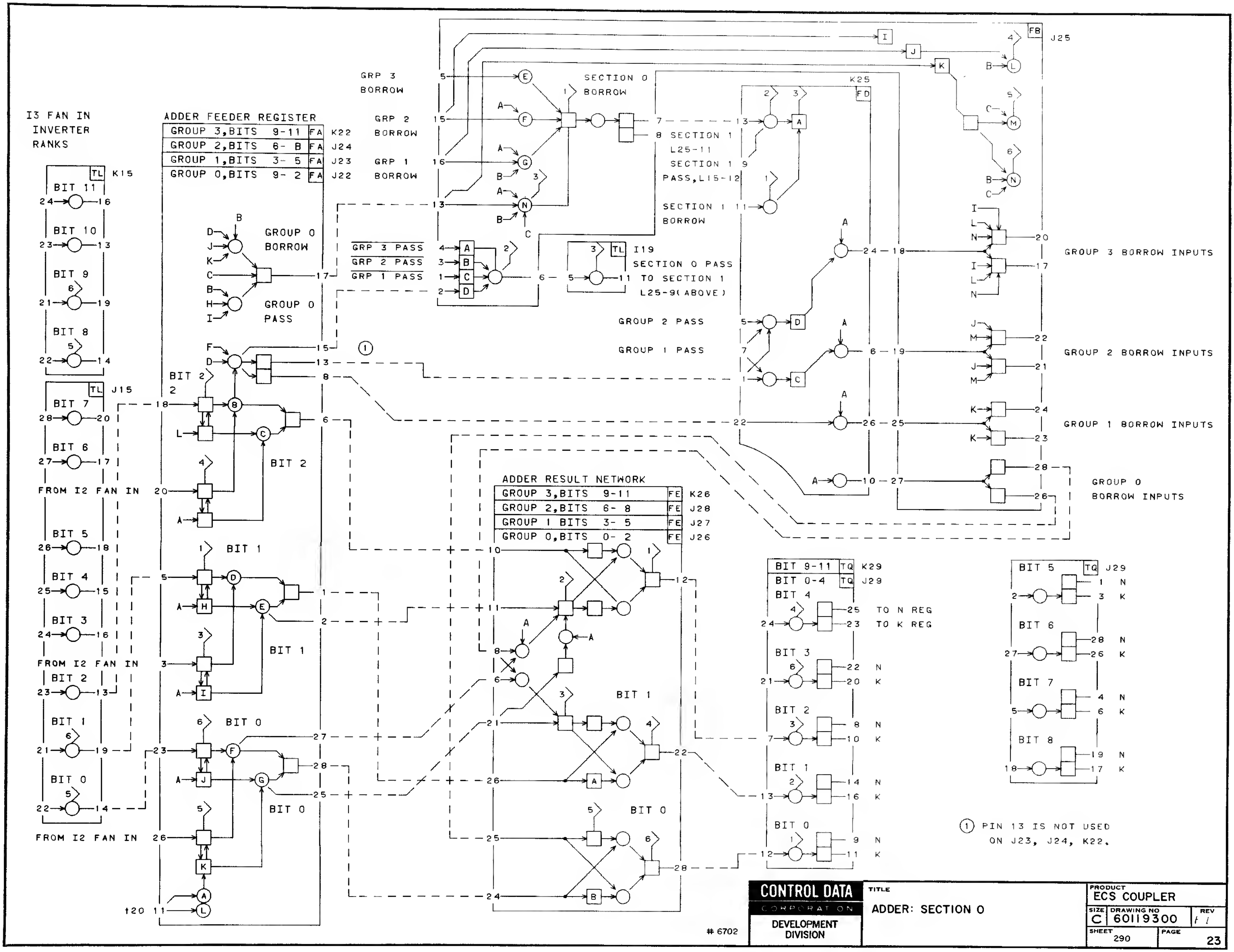
1. SINCE K IS AN 18-BIT REG, BITS 18-23 GO DIRECTLY TO N REG

2. PIN 13 NOT USED ON K24, L22, L23

   PIN 8 NOT USED ON L23

3. THIS ADDER IS IDENTICAL TO THE LONG ADD UNIT IN THE 6600. SEE PUB. NO. 60119300

CONTROL DATA	TITLE	PRODUCT	
DEVELOPMENT DIVISION	ADDER, SECTION I	ECS COUPLER	
		SIZE C, DRAWING NO. 60119300	REV.
		SHEET 289	PAGE 22


I3 FAN IN INVERTER RANKS
ADDER FEEDER REGISTER
GROUP 3, BITS 9-11 FA K22
GROUP 2, BITS 6- 8 FA J24
GROUP 1, BITS 3- 5 FA J23
GROUP 0, BITS 0- 2 FA J22
GROUP 0 BORROW
GROUP 0 PASS
GRP 3 BORROW
GRP 2 BORROW
GRP 1 BORROW
SECTION 0 BORROW
GRP 3 PASS
GRP 2 PASS
GRP 1 PASS
SECTION 1 L25-11
SECTION 1 PASS, L15-12
SECTION 1 BORROW
SECTION 0 PASS TO SECTION 1 L25-9 (ABOVE)
GROUP 2 PASS
GROUP 1 PASS
GROUP 3 BORROW INPUTS
GROUP 2 BORROW INPUTS
GROUP 1 BORROW INPUTS
GROUP 0 BORROW INPUTS
FROM I2 FAN IN
ADDER RESULT NETWORK
GROUP 3, BITS 9-11 FE K26
GROUP 2, BITS 6- 8 FE J28
GROUP 1 BITS 3- 5 FE J27
GROUP 0, BITS 0- 2 FE J26
BIT 9-11 TQ K29
BIT 0-4 TQ J29
TO N REG
TO K REG
(1) PIN 13 IS NOT USED ON J23, J24, K22.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
6702
TITLE ADDER: SECTION 0
PRODUCT ECS COUPLER
SIZE C DRAWING NO 60119300
SHEET 290
PAGE 23

P DECREMENTER AND REGISTER

The output of the decrementer is one count less than the 3-bit quantity in the P register. When the clear/set input to P is strobed at t00, this reduced quantity is entered in P.

The lower 3-bits of K are entered in P unless it is the last record; then the lower 3 bits of B are entered in P.

The decrementer runs only when the Enable P FF is set. On a write operation this is at T41 but on a Read operation there is a considerable delay before the data arrives, so the Read 2 FF is sent through a 300 nsec delay chain before setting the Enable P FF. Once this FF is set, the remainder of the coupler's logic can start the next Record Setup and the clock pulses decrement P and send the GO signal to the Exchange Address Counter. When P = 0 the Enable P FF will be cleared unless a new request has been sent; that is, it was not the last record. Note that the decrementer logic is cyclic; it will decrement an all zero P register to all ones.

LAST RECORD CONTROL

WORD COUNT ≤ FLIP FLOP

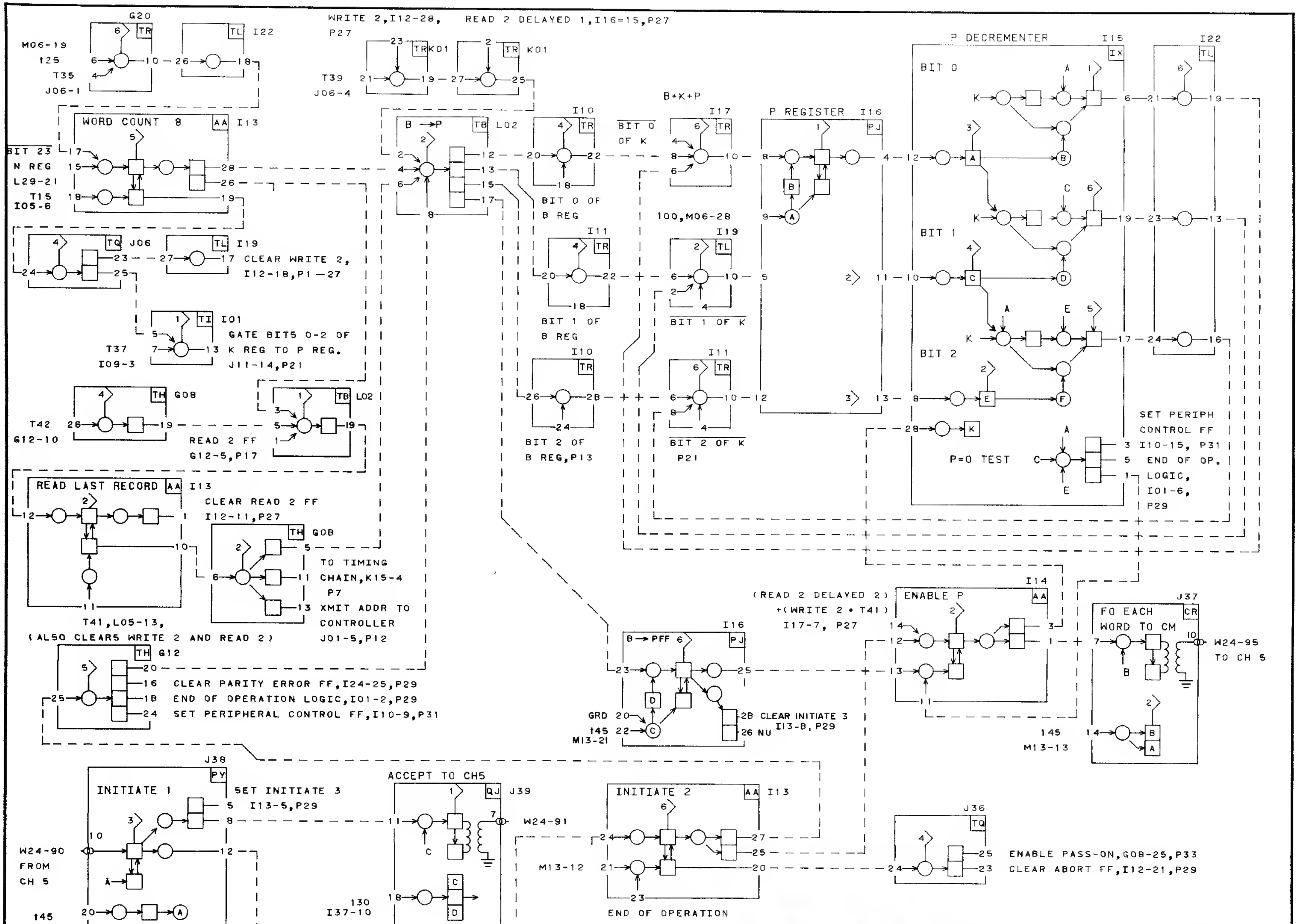
This is set if the N register is positive after the K-B check. If set, B is sent to P; if clear, K is sent to P.

READ LAST RECORD FLIP FLOP

This is set by the Word Count ≤ 8 FF, Read 2 FF and T42 and blocks the reset Record Setup sequence from occurring.

INITIATE 1 FLIP FLOP

This is set from CPU when the instruction is translated. The Accept signal is returned immediately to CPU.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

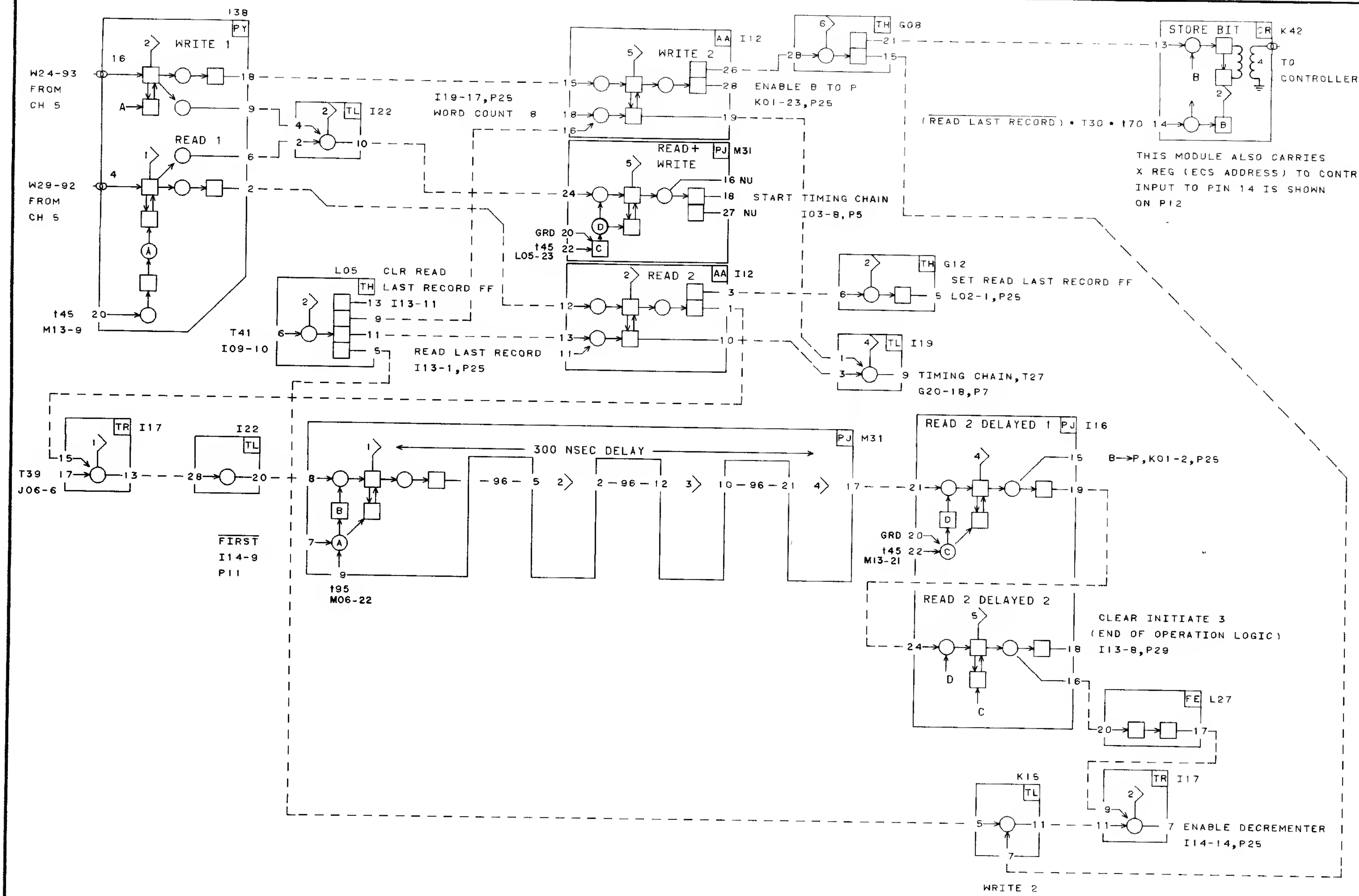
TITLE
P DECREMENTER AND REGISTER
GO TO CM
INITIATE/ACCEPT FROM CH 5

PRODUCT		
ECS COUPLER		
SIZE C	DRAWING NO 60119300	REV
SHEET 291		PAGE 25

READ AND WRITE FF DESCRIPTIONS

Along with the Initiate 1 signal, CPU sets either the Write 1 or Read 1 FFs. The Read/Write FF is set by either one and the timing chain started. On a Read operation the decrementer is not enabled until T39 + 400 nsec to give the data time to reach the coupler. On a Write operation, the delay is not necessary.

When the last record reaches T42 and tries to restart at T27, the timing chain will be blocked. Either Write 2 or Read 2 must be set for it to continue.



\# 6704

CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

TITLE: READ AND WRITE FFS

PRODUCT: ECS COUPLER

SIZE: C DRAWING NO: 60119300 REV

SHEET: 292 PAGE: 27

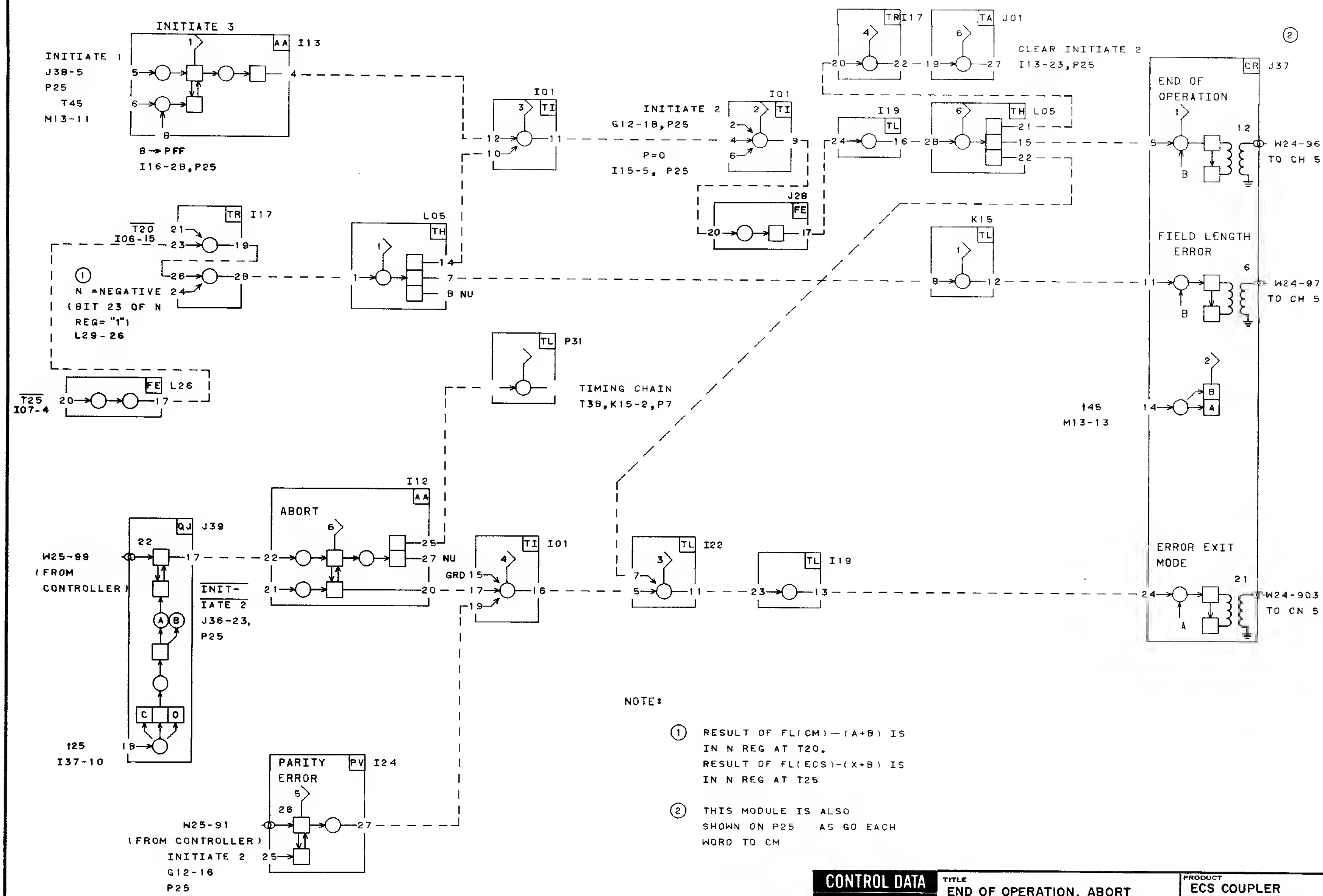
ERROR AND TERMINATION CONDITIONS

End of Operation signal is sent if the decrementer reaches 0 and this is the last record, or if a Field Length error occurs.

A Field Length error signal is sent after checking FL(CM)-(A+B) and FL(ECS)-(X+B) and getting a negative result. This is the only error condition that the coupler checks or acts upon.

Error Exit Mode signal is sent on any Field Length error, Abort or Parity error. Note that CPU cannot distinguish between a Parity Error and an Abort.

On a Read Operation, an Abort is used in place of the Accept to keep the timing chain running. This allows the programmer to transfer all zeroes to CM if he wishes. On a Write Operation CPU discontinues the transfer. On a Parity Error, the coupler relays the signal as an Error Exit Mode. Neither Abort nor Parity Error cause an End of Operation signal.

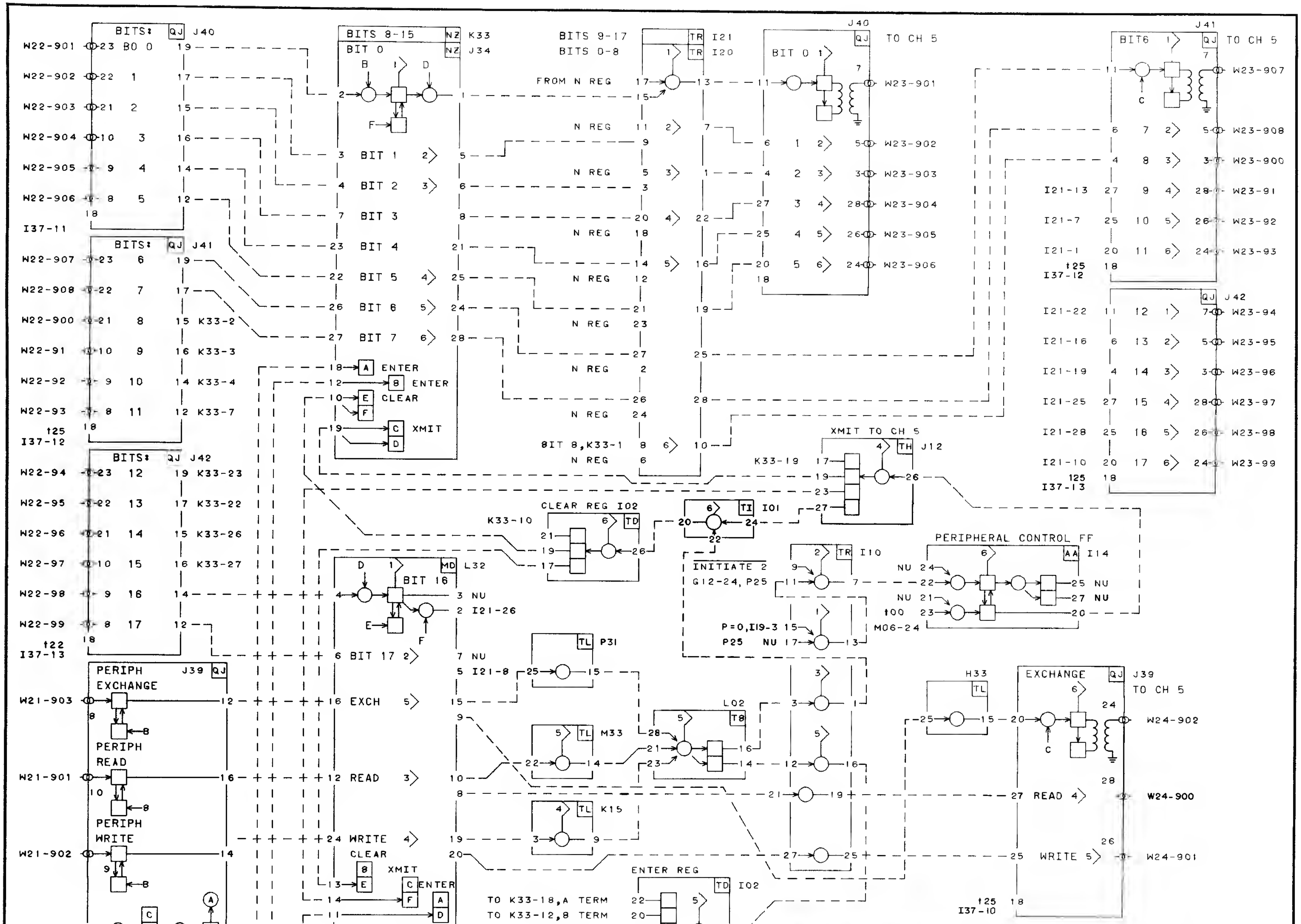


NOTE:

1. RESULT OF FL(CM)—(A+B) IS IN N REG AT T20. RESULT OF FL(ECS)-(X+B) IS IN N REG AT T25
2. THIS MODULE IS ALSO SHOWN ON P25 AS GO EACH WORD TO CM

#6705

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE END OF OPERATION, ABORT PARITY ERROR, FIELD LENGTH ERROR	PRODUCT ECS COUPLER	
		SIZE C DRAWING NO 60119300	REV.
		SHEET 293	PAGE 29



#6706

CONTROL DATA CORPORATION

DEVELOPMENT DIVISION

TITLE

PERIPHERAL ADDRESS NETWORK (TO CM)

PRODUCT ECS COUPLER

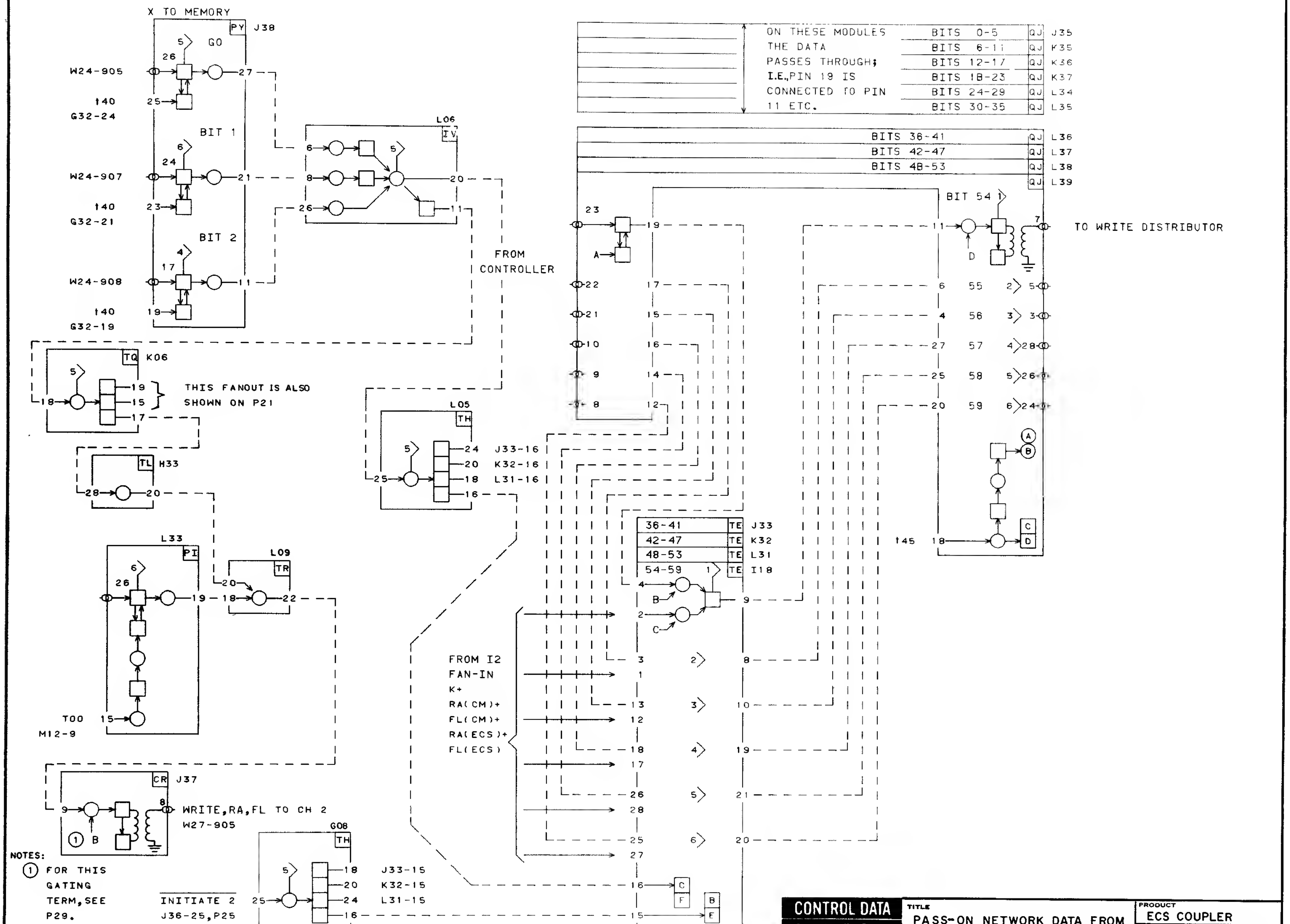
SIZE C DRAWING NO 60119300 REV

SHEET 294 PAGE 31

PASS-ON NETWORK DESCRIPTION

The data path from the Controller to CM has provision for the contents of the Coupler's registers to be restored into memory. This logic is the OR gate marked on the block diagram and provides a restore path for RA(ECS) and FL(ECS) if an Exchange Jump is executed. RA(CM) and FL(CM) are restored from the CPU. As long as the coupler is involved in a data transfer, the data path from the Controller to the Write Distributor (Chassis 2) is enabled. This is done by the Initiate 2 FF, which is cleared only on an End of Operation condition.

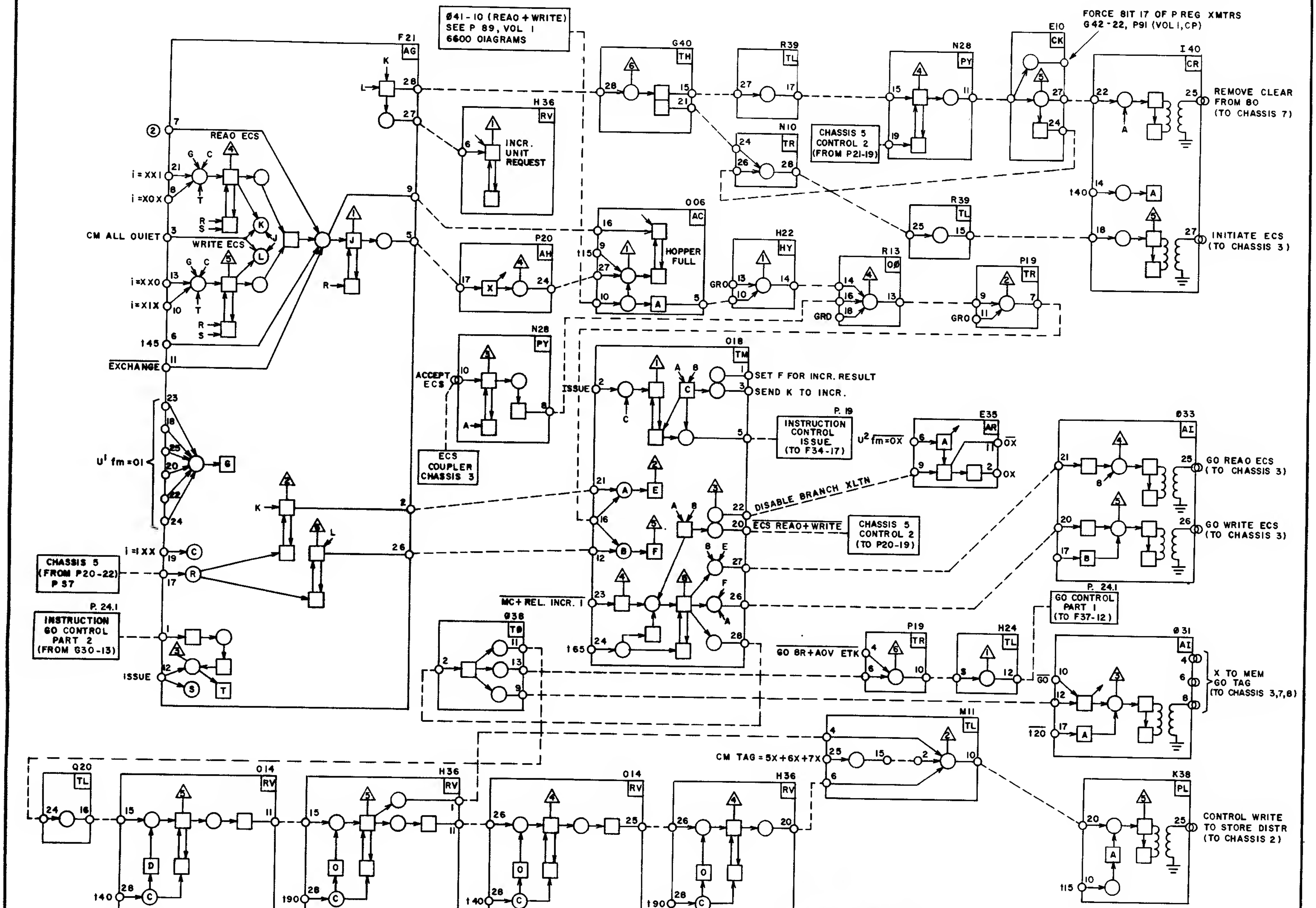
The address tags from the stunt box are translated for an Exchange Jump and enable RA(ECS) and FL(ECS) to be stored in Exchange Jump packet. (Note that bit 1 of these tags is also used; see I2 fan in, page 21.) It is not necessary to restore the CM parameters, as these also held on the CPU and restored from there.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: PASS-ON NETWORK DATA FROM CONTROLLER TO CM AND RESTORE PATHS FOR EXCHANGE JUMP

PRODUCT: ECS COUPLER
SIZE: C DRAWING NO: 60119300 REV: F L
SHEET: 295 PAGE: 33

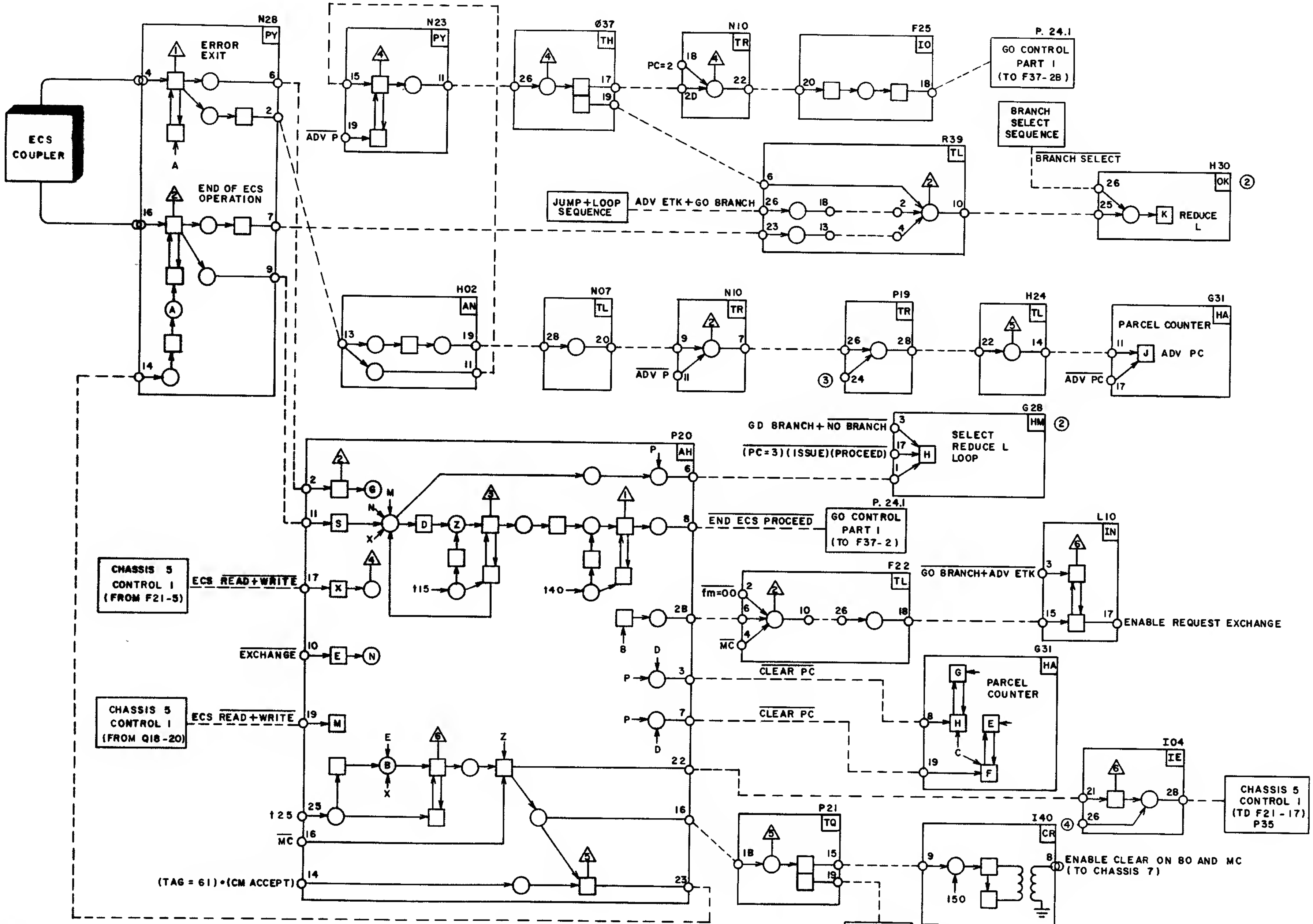


NOTES:

1. ALL LOCATIONS ON CHASSIS 5.

② $\overline{\text{SKIP 1}}\cdot(\text{ISSUE})(\overline{\text{SKIP 1}})\cdot(50+51+52+60+61+62+70+71+72)$.

CONTROL DATA	TITLE: CHASSIS 5, CONTROL 1
DEVELOPMENT DIVISION	PRODUCT: ECS COUPLER
SIZE: C	DRAWING NO: 60119300
REV: B L	SHEET: 296
PAGE: 35	



NOTES:

1. ALL LOCATIONS ON CHASSIS 5.
2. ② SEE FUNCTIONAL UNIT DRAWING ON P. 5 FOR DETAIL.
3. ③ $\overline{\text{SCBD ISSUE}}$ • fm = 0X
4. ④ EXCHANGE P18-19, PAGE 90.1.

CONTROL DATA	TITLE	PRODUCT: ECS COUPLER
DEVELOPMENT DIVISION	CHASSIS 5, CONTROL 2	SIZE: C — DRAWING NO: 60119300 — REV: BL
		SHEET: 297 — PAGE: 37

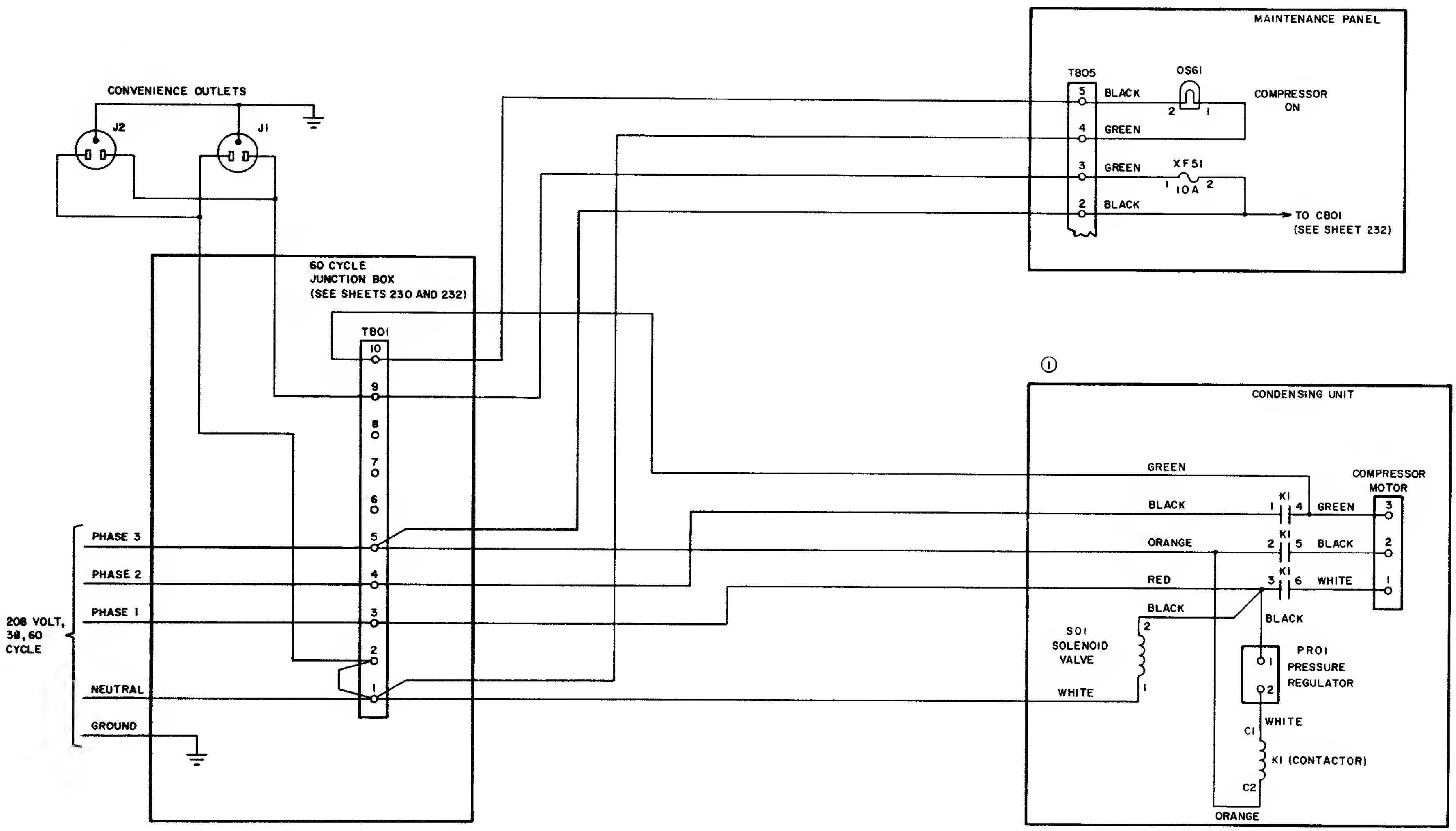
POWER WIRING
CONTENTS

Pub. No. 60119300

Rev. BD

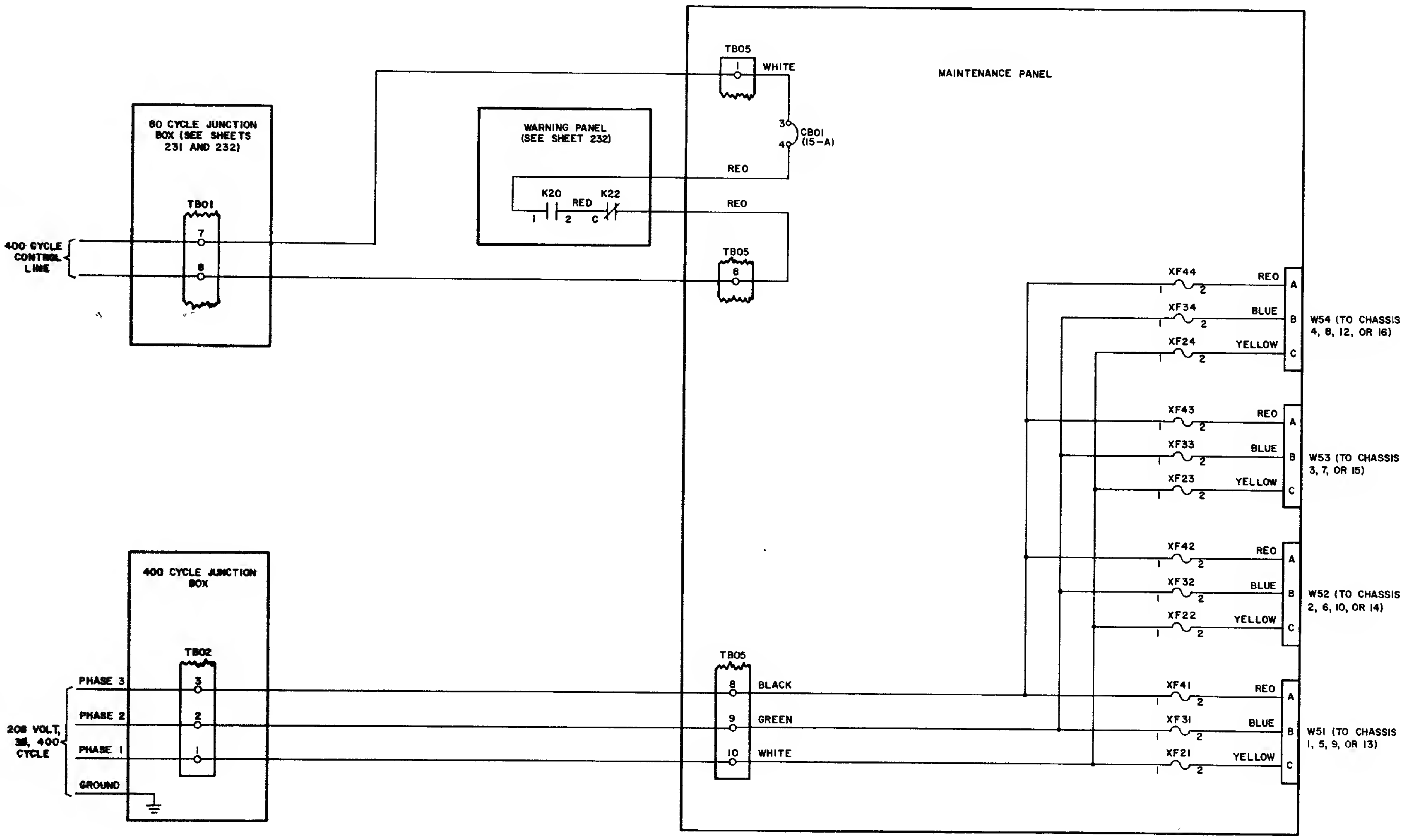
NOTES

(1) TO INSTALL A "C" SERIES CONDENSING UNIT IN PLACE OF AN "A" SERIES CONDENSING UNIT, CHANGE THE WIRES NORMALLY ROUTED FROM THE CONDENSING UNIT TO A3TB2 PINS 2,3,4,& 6 (SHOWN ON PAGE 25) TO TB01 PINS 3,4,5,& 10, RESPECTIVELY. ALSO CHANGE THE WIRES NORMALLY ROUTED FROM THE CONDENSING UNIT TO A3TB3 PINS 3 & 4 TO TB01 PINS 2 & 3, RESPECTIVELY. ALL OTHER WIRING REMAINS THE SAME AS THAT OF THE "A" SERIES CONDENSING UNIT SHOWN ON THIS PAGE.



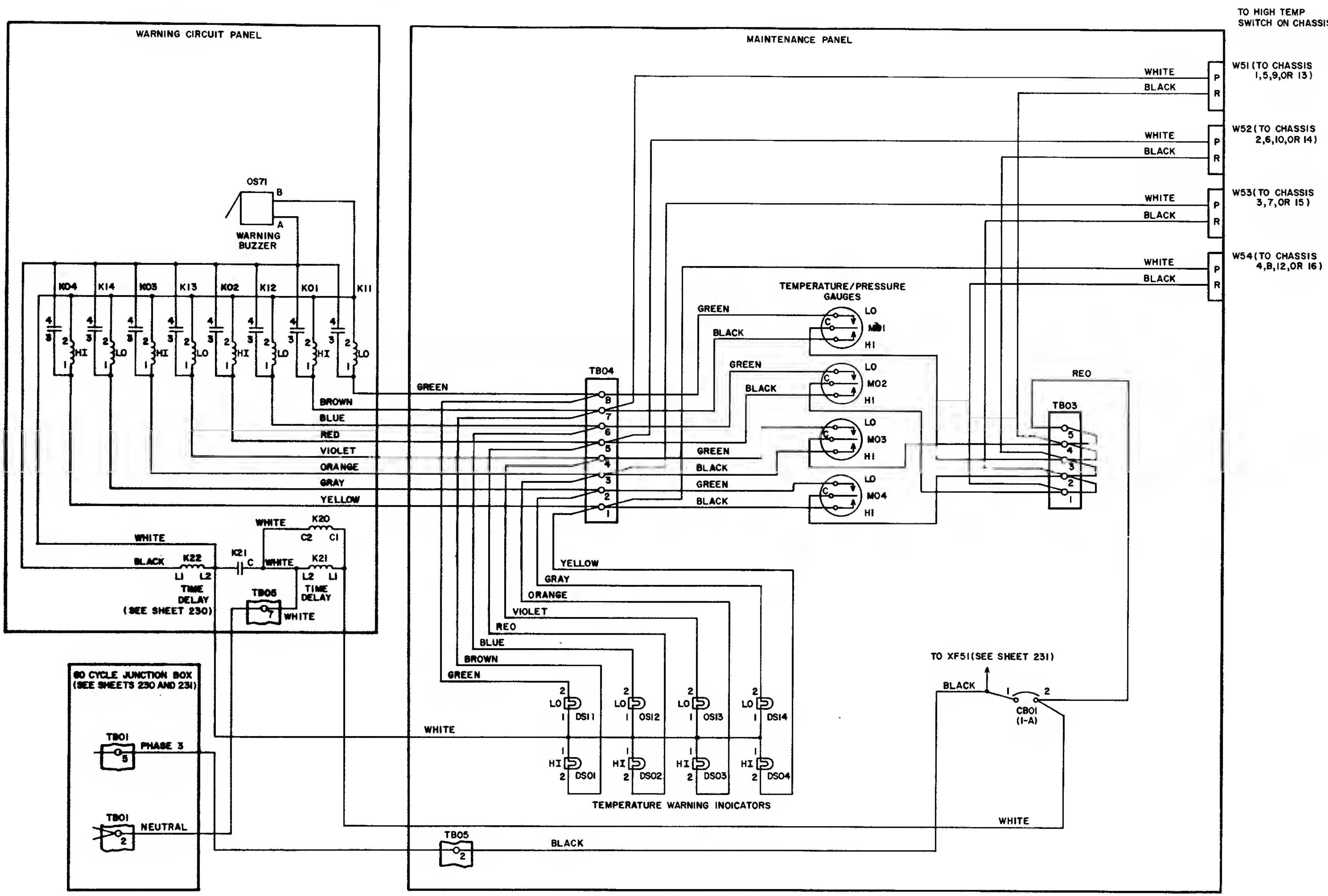
NOTE:
A 6601 CONTAINS 4 SUCH CIRCUITS (ONE PER WING) AND A 6604 CONTAINS 3.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE 6600 CENTRAL COMPUTER 60 CYCLE POWER WIRING, CONDENSING UNIT AND CONVENIENCE OUTLETS	PRODUCT 6601/04 SIZE C · DRAWING NO 60119300 · REV H SHEET 231 · PAGE 1



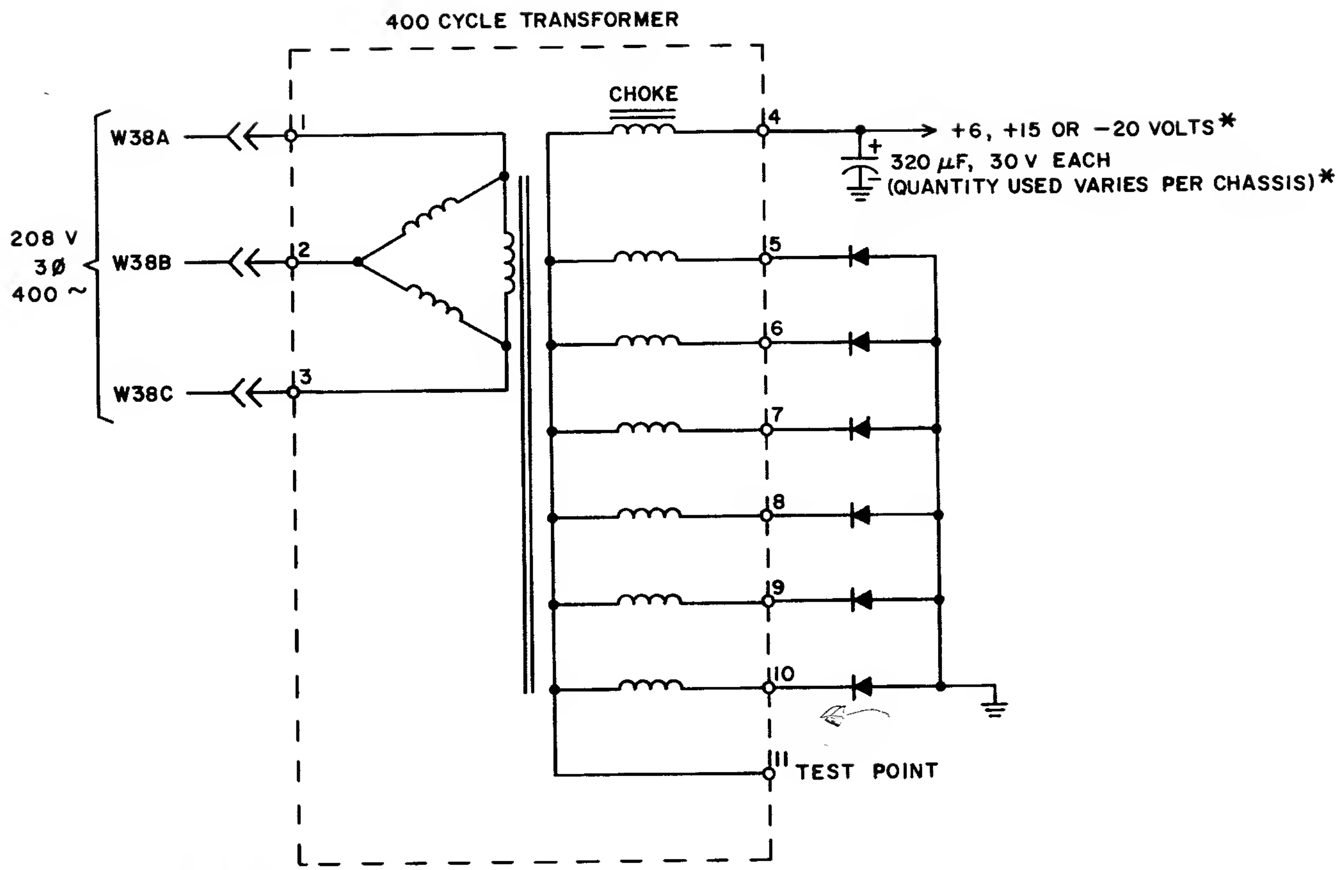
NOTE:
A 6601 CONTAINS 4 SUCHS CIRCUITS (ONE PER WING) ANO A 6604 CONTAINS 3.

CONTROL OATA CORPORATION COMPUTER DIVISION	TITLE 6600 CENTRAL COMPUTER 400 CYCLE POWER WIRING AND CONTROL	PRODUCT 6601/04 SIZE C · DRAWING NO. 60119300 · REV K SHEET 230 · PAGE 3



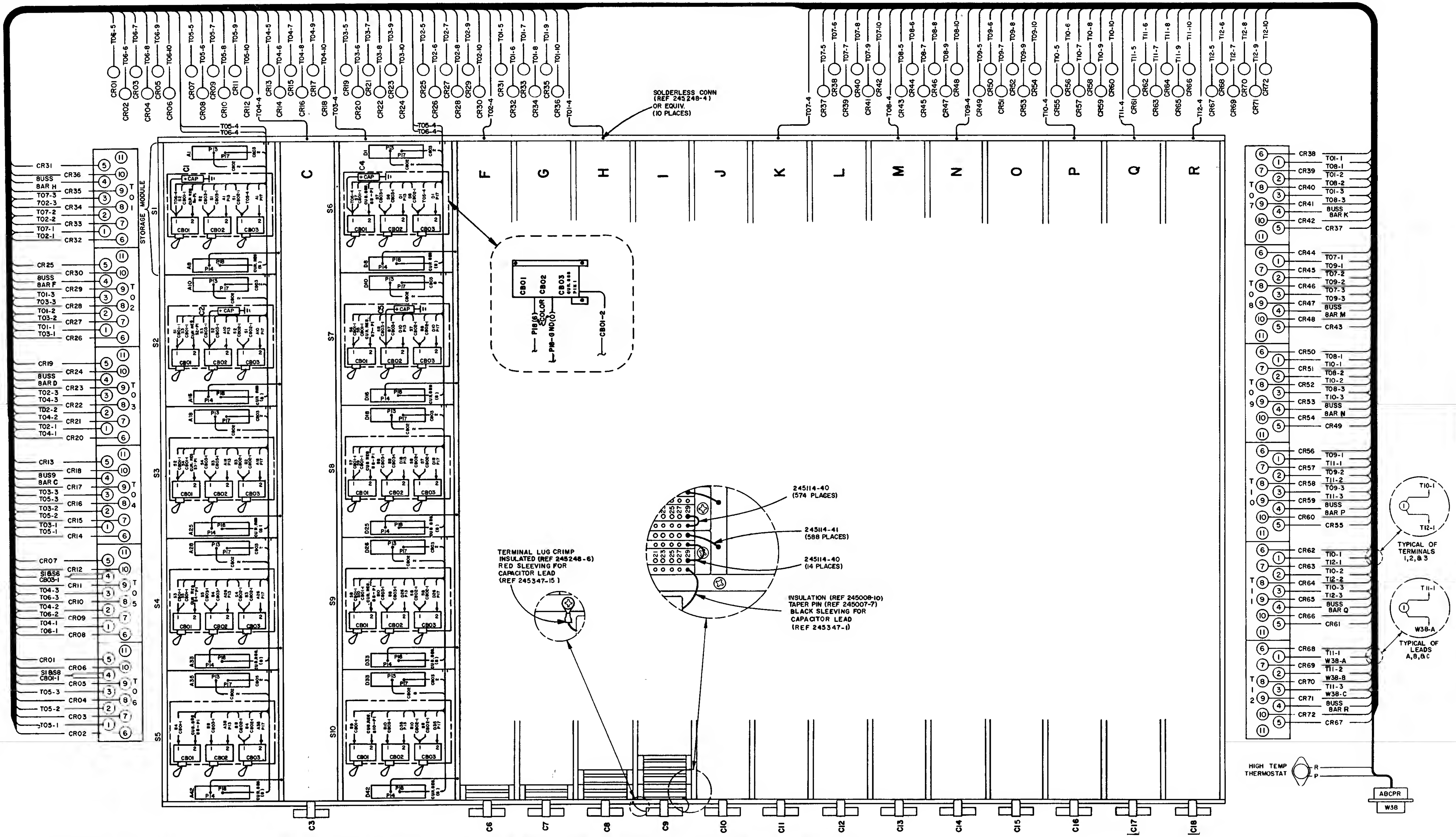
NOTE:
A 6601 CONTAINS 4 SUCH CIRCUITS (ONE PER WING) AND A 6604 CONTAINS 3.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE 6600 CENTRAL COMPUTER 60 CYCLE POWER WIRING WARNING CIRCUIT	PRODUCT 6601/04 SIZE C DRAWING NO. 60119300 REV K	SHEET 232 PAGE 5



* DIODES AND CAPACITORS ARE REVERSED FOR −20 VOLT POWER SUPPLIES.

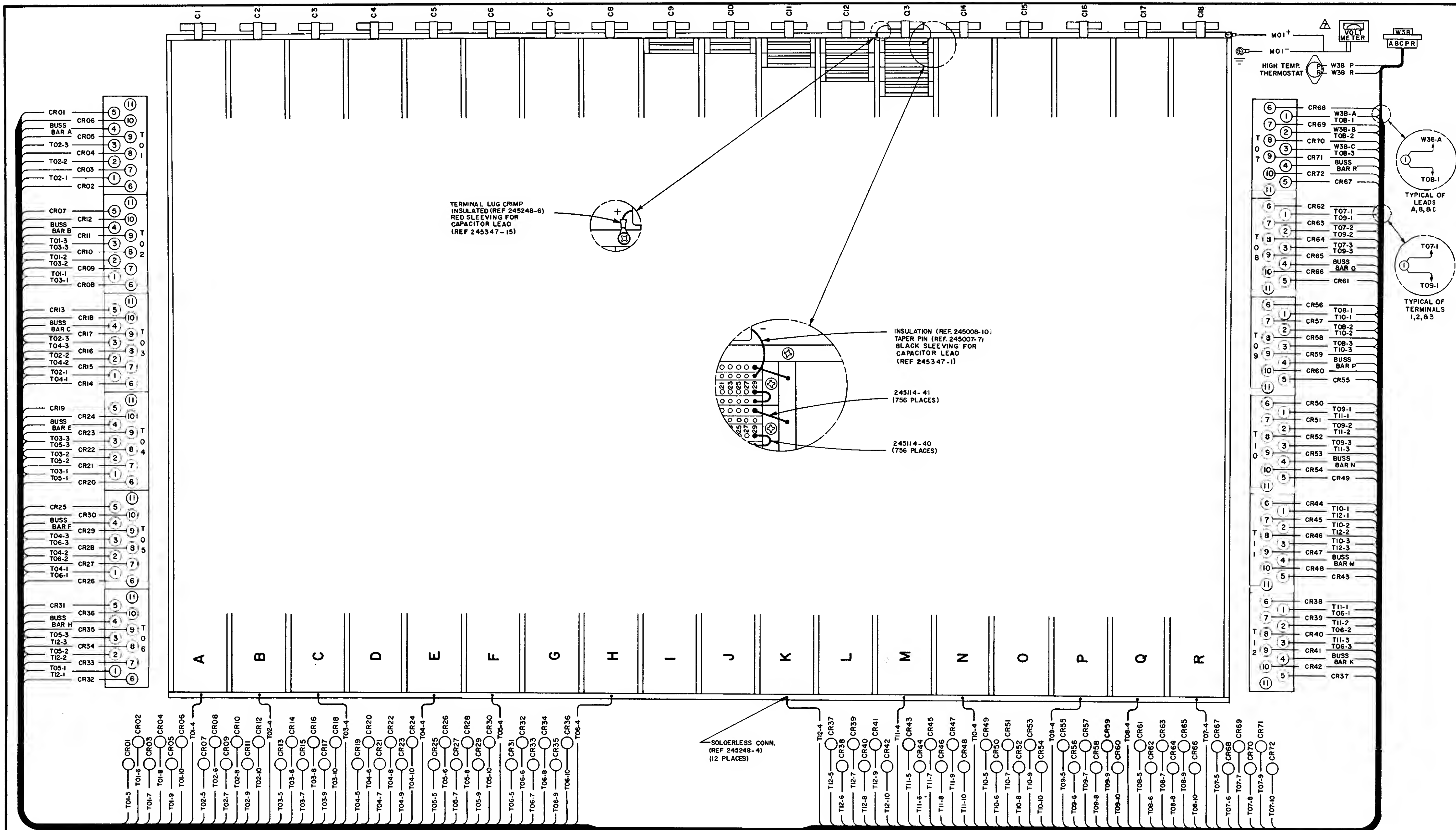
TYPICAL 6, 15, OR −20 VOLT
POWER SUPPLY



NOTES:

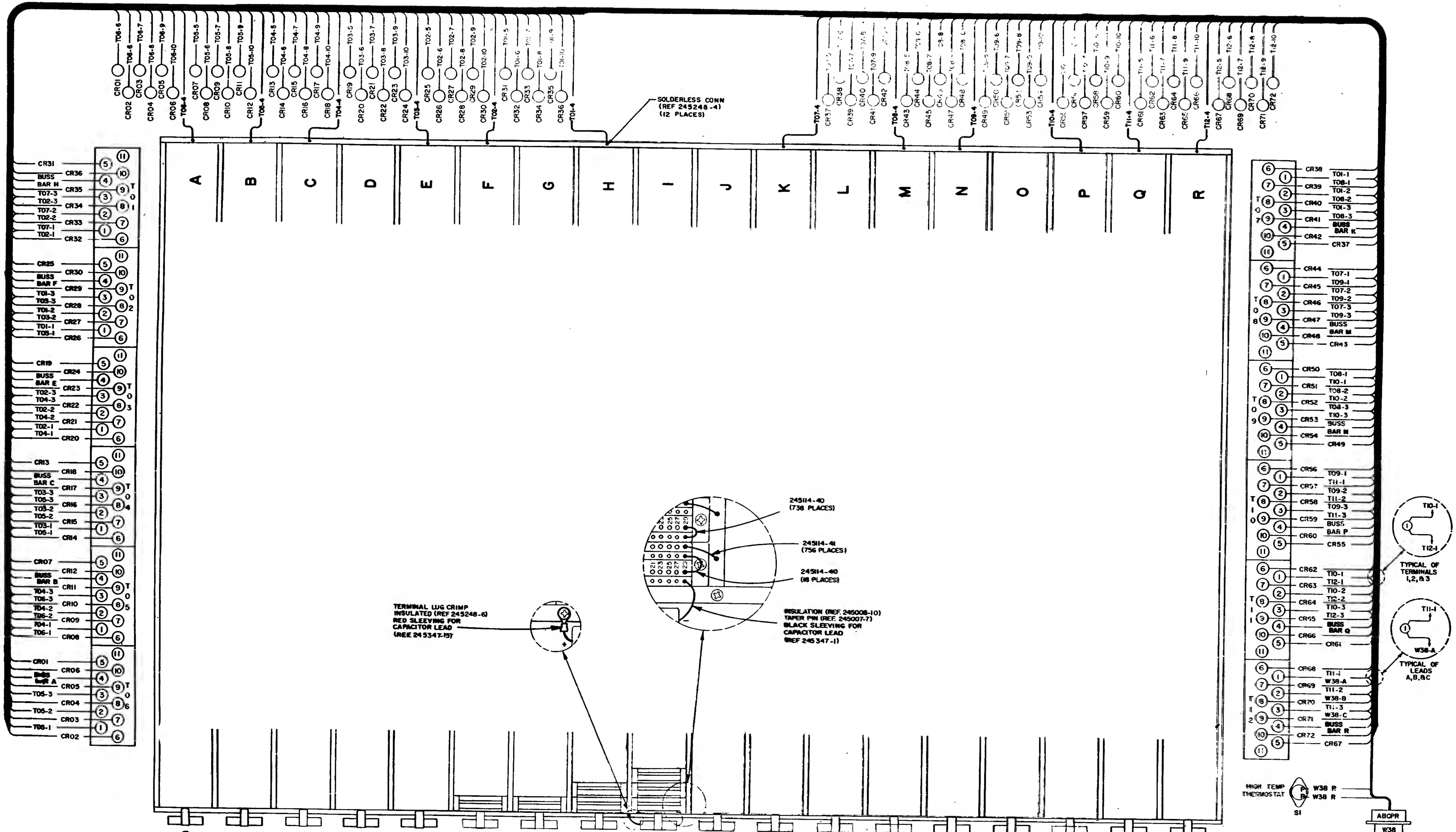
1. FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 63D25200.
2. ALL POWER-IN WIRING (W38-A, ETC.) MUST BE 18AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-87. POWER WIRING TO BUSS BARS & RECTIFIERS FROM T01-T04 & T07-T12 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-143. POWER WIRES FROM T05-4, MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP. 245483-117. POWER WIRES FROM T06-4, MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP. 245483-119. POWER WIRING FROM T05-5,6,7,8,9&10 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-145 POWER WIRING FROM T06-5,6,7,8,9&10 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-147. POWER WIRING FROM CB01-2 (10 PLACES) MUST BE 18 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-91. POWER WIRING FROM CB02-2 & CB03-2 (10 PLACES) MUST BE 18 AWG STRANDED INS WIRE PER CONTROL DATA CORP 245483-89 POWER WIRE P14 TO BUSS-BAR (10 PLACES) MUST BE 18 AWG STRANDED INS WIRE PER CONTROL DATA CORP 245483-87
3. USE TAPER PIN (REF 245007-2) & INSULATION (REF 245523-37) FOR CONNECTIONS P18, P13, P17, & BOTH ENDS OF P14 TO BUSS BAR.
4. TRANSFORMERS T01-T05 & T07-T12 ARE 970101 (+6V) TRANSFORMERS T06 IS 18119900 (+15 V)
5. BUSS-BAR CAPACITOR POLARITY: + TO BUSS-BAR. − TO CONNECTOR.
6. CAPACITORS MOUNTED WITHIN THE CIRCUIT BREAKER ARE MOUNTED WITH THE + LEAD SOLDERED TO PIN 1 OF THE CORRESPONDING CIRCUIT BREAKER AND THE NEGATIVE LEAD IS FASTENED TO AN ADJACENT MOUNTING SCREW BY A SOLDER LUG, (REF 8177) OR EQUIV THE CAPACITOR LEADS ARE COVERED WITH TUBING AS SPECIFIED FOR THE BUSS-BAR CAPACITORS.
7. USE CAPACITOR (REF 245072-37) & RECTIFIERS (REF 24561602)
8. FOR WIRE LISTING SEE 63762500

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE POWER WIRING CHASSIS 1	PRODUCT 6601/6604/6613/6614
		SIZE D DRAWING NO. 60119300 REV. BD
		SHEET PAGE 7



NOTES
1. FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 63025300.
2. ALL POWER-IN WIRING (W38-A, ETC.) MUST BE 18AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-87
ALL POWER WIRING TO BUSS BARS & RECTIFIERS MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-143
3. TRANSFORMERS T01-T12 ARE 970101 (+6 VOLT).
4. CAPACITOR POLARITY: + TO BUSS BAR (REF 245072-37) – TO CONNECTOR
5. RECTIFIERS ARE (REF 24561602)
6. FOR WIRE LISTING SEE 63762600
7. VOLTMETER LEADS WILL BE INSTALLED ONLY ON CHASSIS B, 63025304.

CONTROL DATA DEVELOPMENT DIVISION	TITLE EVEN LOGIC CHASSIS POWER WIRING CHASSIS 2, 6, B	PRODUCT 6601/6604/6613/6614 SIZE C · DRAWING NO. 60119300 · REV. B0 SHEET · PAGE 9



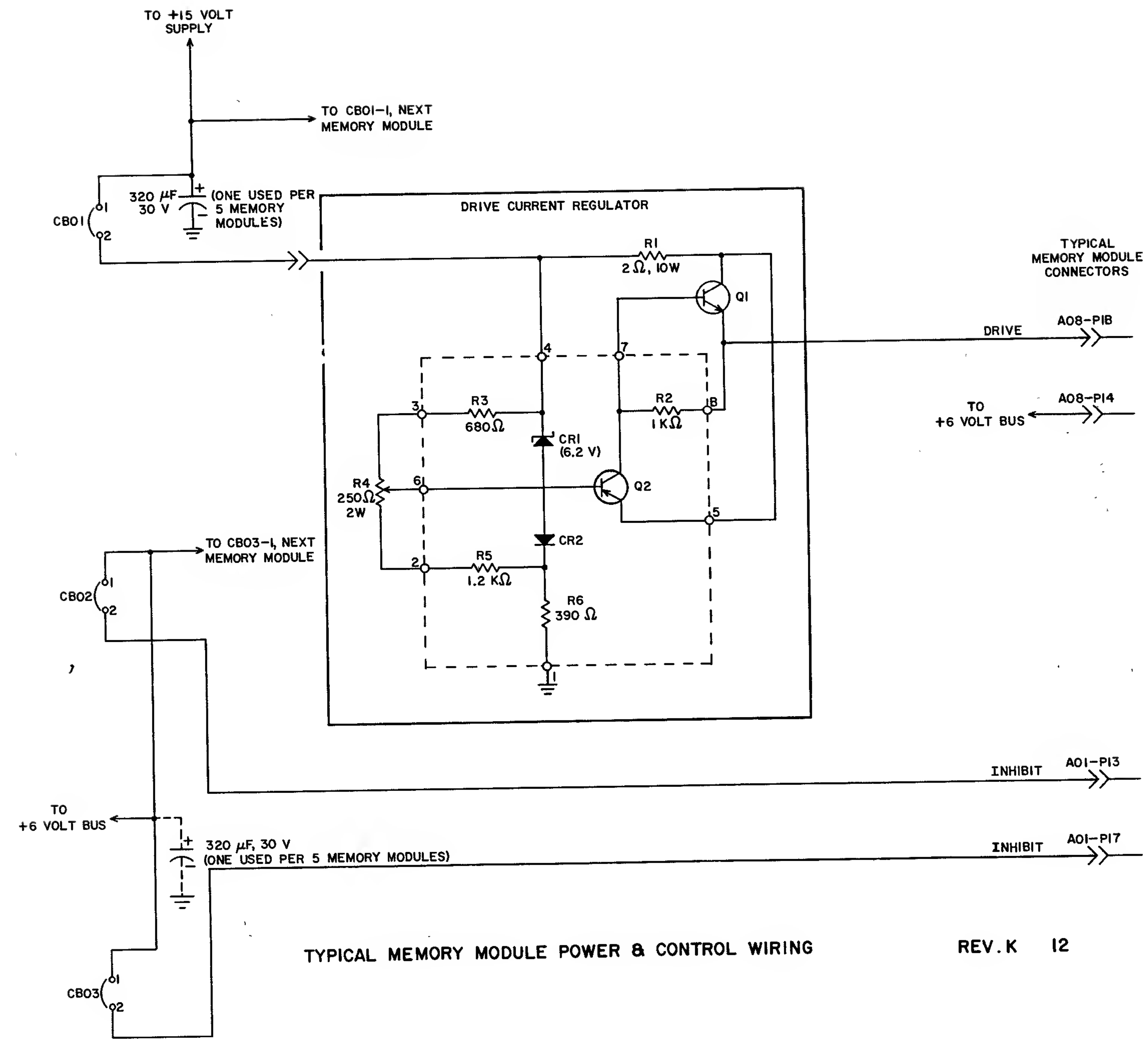
NOTES:

1. FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 63025300.
2. ALL POWER-IN WIRING (W38-A, ETC.) MUST BE [illegible], STRANDED INS WIRE PER CONTROL DATA CORP 245483-87. ALL POWER WIRING TO BUSS BARS & RECTIFIERS MUST BE 14 AWG, STRD. INS. WIRE PER CONTROL DATA CORP. 245483-143.
3. TRANSFORMERS T01-T12 ARE 970101 (+6 VOLT).
4. CAPACITOR POLARITY: + TO BUSS BAR (REF 245072-37) – TO CONNECTOR.
5. USE RECTIFIERS (REF 24561602).
6. FOR WIRE LISTING SEE 63762700.

B-60119300

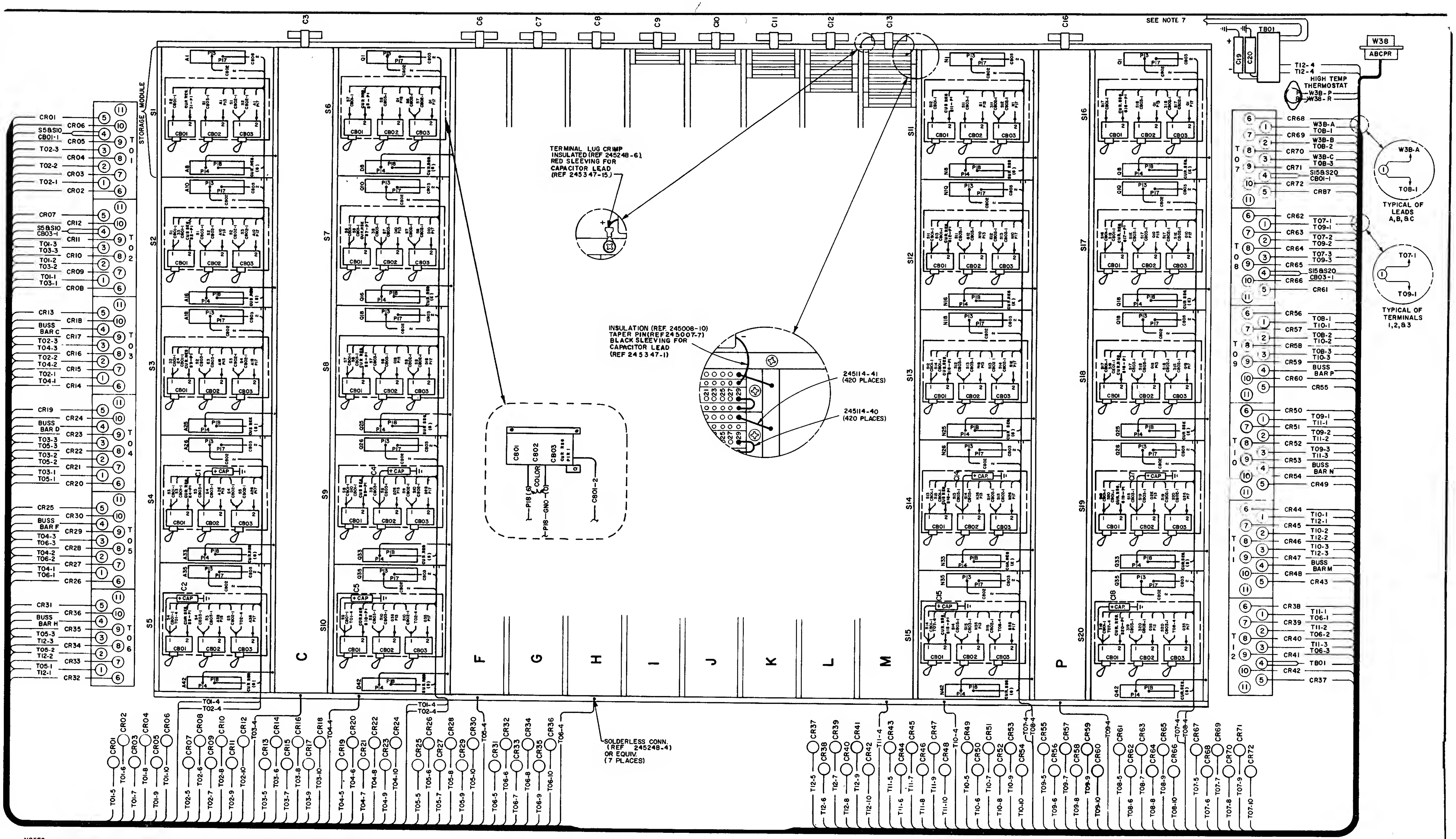
ODD LOGIC CHASSIS
POWER WIRING
CHASSIS 5 AND 7

REV. K 11



TYPICAL MEMORY MODULE POWER & CONTROL WIRING

REV. K 12



NOTES

1 FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 63025200

2 ALL POWER-IN WIRING (W 38-A,ETC,) MUST BE 18 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-87 POWER WIRING TO BUSS-BARS & RECTIFIERS FROM T03-T06 & T09-T11 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-143 POWER WIRES FROM T02-4 & T08-4 MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-117 POWER WIRES FROM T01-4 & T07-4, MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-119 POWER WIRES FROM T12-4, MUST BE 18 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-91 POWER WIRING FROM T01 & T07-5,6,7,8,9 & 10 MUST BE 14 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-147 POWER WIRING FROM T02 & T08-5,6,7,8,9 & 10 MUST BE 14 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-145 POWER WIRING FROM T12-5,6,7,8,9 & 10 MUST BE 14 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-147 POWER WIRING FROM CB01-2 (20 PLACES) MUST BE 18 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-91 POWER WIRING FROM CB02-2 & CB03-2 (20 PLACES) MUST BE 18 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-89 POWER WIRE P14 TO BUSS-BAR (20 PLACES) MUST BE 18 AWG STRANDED INS WIRE PER CONTROL DATA CORP 245483-87

3. USE TAPER PIN (REF 245007-2) & INSULATION (REF 245523-37). FOR CONNECTIONS P18,P13,P17 & BOTH ENDS OF P14 TO BUSS-BAR

4. TRANSFORMERS T02-T06 & T08-T11 ARE 970101 (+6V) TRANSFORMERS T01 & T07 ARE 18119900 (+15V) TRANSFORMER T12 IS 100043 (-20V).

5 BUSS BAR CAPACITORS POLARITY + TO BUSS-BAR. - TO CONNECTOR.

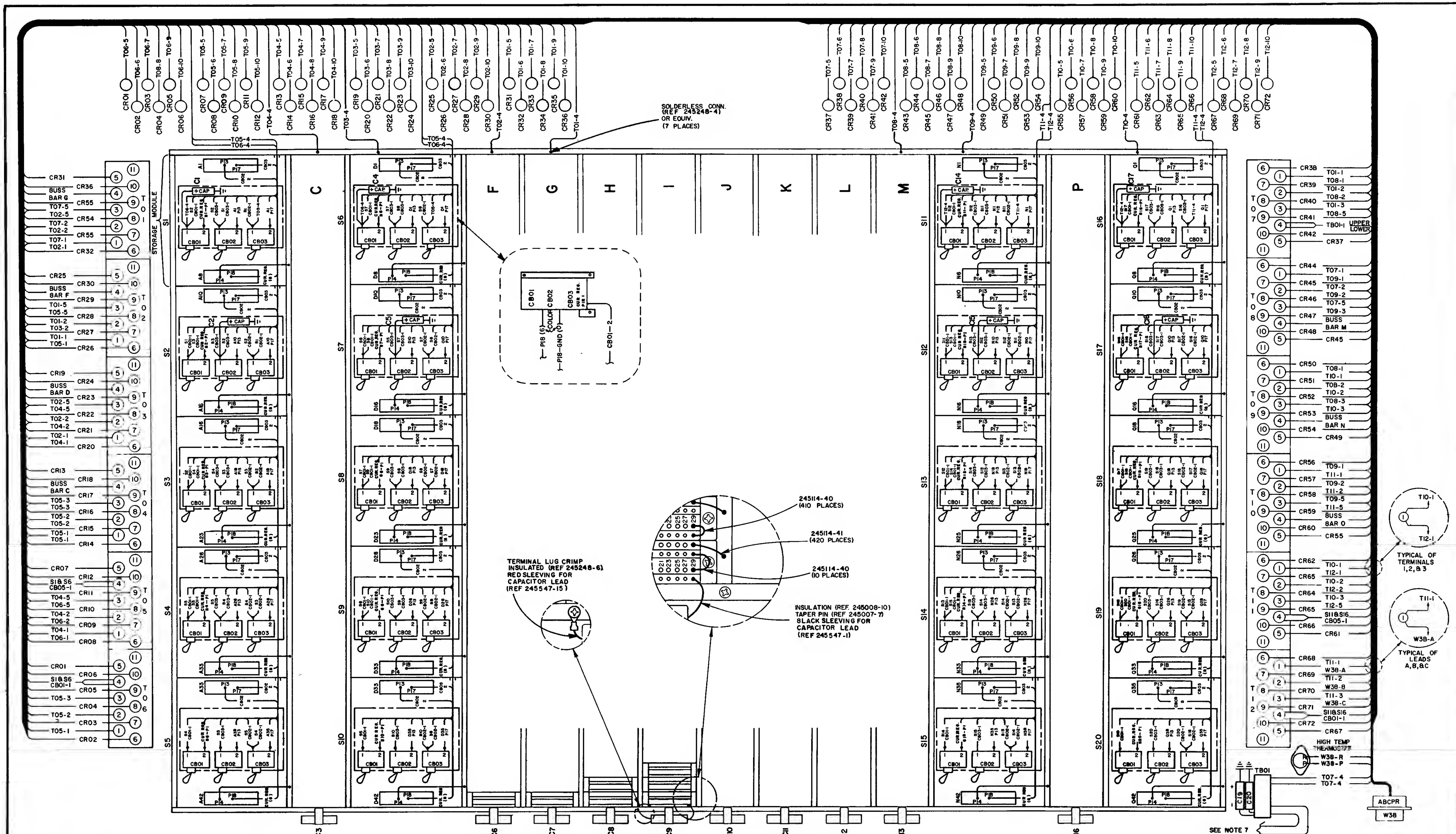
6. CAPACITORS MOUNTED WITHIN THE CIRCUIT BREAKER ARE MOUNTED WITH THE + LEAD SOLDERED TO PIN 1 OF THE CORRESPONDING CIRCUIT BREAKER AND THE NEGATIVE LEAD IS FASTENED TO AN ADJACENT MOUNTING SCREW BY A SOLDER LUG, (REF 8177) OR EQUIV. THE CAPACITOR LEADS ARE COVERED WITH TUBING AS SPECIFIED FOR THE BUSS-BAR CAPACITORS.

7. -20V JUMPER WIRES MUST BE 18AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-91. THE NUMBER AND LOCATION OF THE -20V JUMPERS ARE DETERMINED BY THE APPROPRIATE SYNCHRONIZER TABS.

8. CAPACITORS ARE (REF 245072-37) & RECTIFIER CR01 THRU CR36 & CR43 THRU CR72 ARE (REF 24561602) & CR37 THRU CR42 ARE (REF 24561601)

9 FOR WIRE LISTING SEE 63762800

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE POWER WIRING EVEN MEMORY CHASSIS	PRODUCT 6601/6604/6613/6614
		SIZE C — DRAWING NO 60119300 — REV. BD
		SHEET — PAGE 13



NOTES

1 FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 65025200

2 ALL POWER-IN WIRING (W58-A, ETC.) MUST BE 18 AWG, STANDARD INS WIRE PER CONTROL DATA CORP 245483-87
POWER WIRING TO BUSS BARS & RECTIFIERS.
FROM T01-T04 & T06-T10 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-143
POWER WIRES FROM T05-4 & T11-4, MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-117
POWER WIRES FROM T06-4 & T12-4, MUST BE 16 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-119
POWER WIRES FROM T07-4, MUST BE 18 AWG, STRANDED INS WIRE PER CONTROL DATA CORP. 245483-91
POWER WIRING FROM T06 & T12-5,6,7,8,9 & 10 MUST BE 14 AWG STRANDED INS WIRE PER CONTROL DATA CORP 245483-147
POWER WIRING FROM T05 & T11-5,6,7,8,9 & 10 MUST BE 14 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-145
POWER WIRING FROM T07-5,6,7,8,9 & 10 MUST BE 14 AWG, STRD. INS WIRE PER CONTROL DATA CORP. 245483-147
POWER WIRING FROM CB01-2 (20 PLACES) MUST BE 18 AWG, STRD INS WIRE PER CONTROL DATA CORP. 245483-91
POWER WIRING FROM CB02-2 & CB05-2 (20 PLACES) MUST BE 18 AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-89
POWER WIRE P14 TO BUSS-BAR (20 PLACES) MUST BE 18 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245485-87

5. USE TAPER PIN (REF. 245007-2) & INSULATION (REF. 245523-37), FOR CONNECTIONS P18, P13, P17 & BOTH ENDS OF P14 TO BUSS BAR.

4 TRANSFORMERS T01-T05 & T08-T11 ARE 970101. (+6V) TRANSFORMERS T06 & T12 ARE 18119900 (+15V), TRANSFORMERS T07 IS 100043 (-20V).

5. BUSS-BAR CAPACAITOR POLARITY: + TO BUSS-BAR. - TO CONNECTOR.

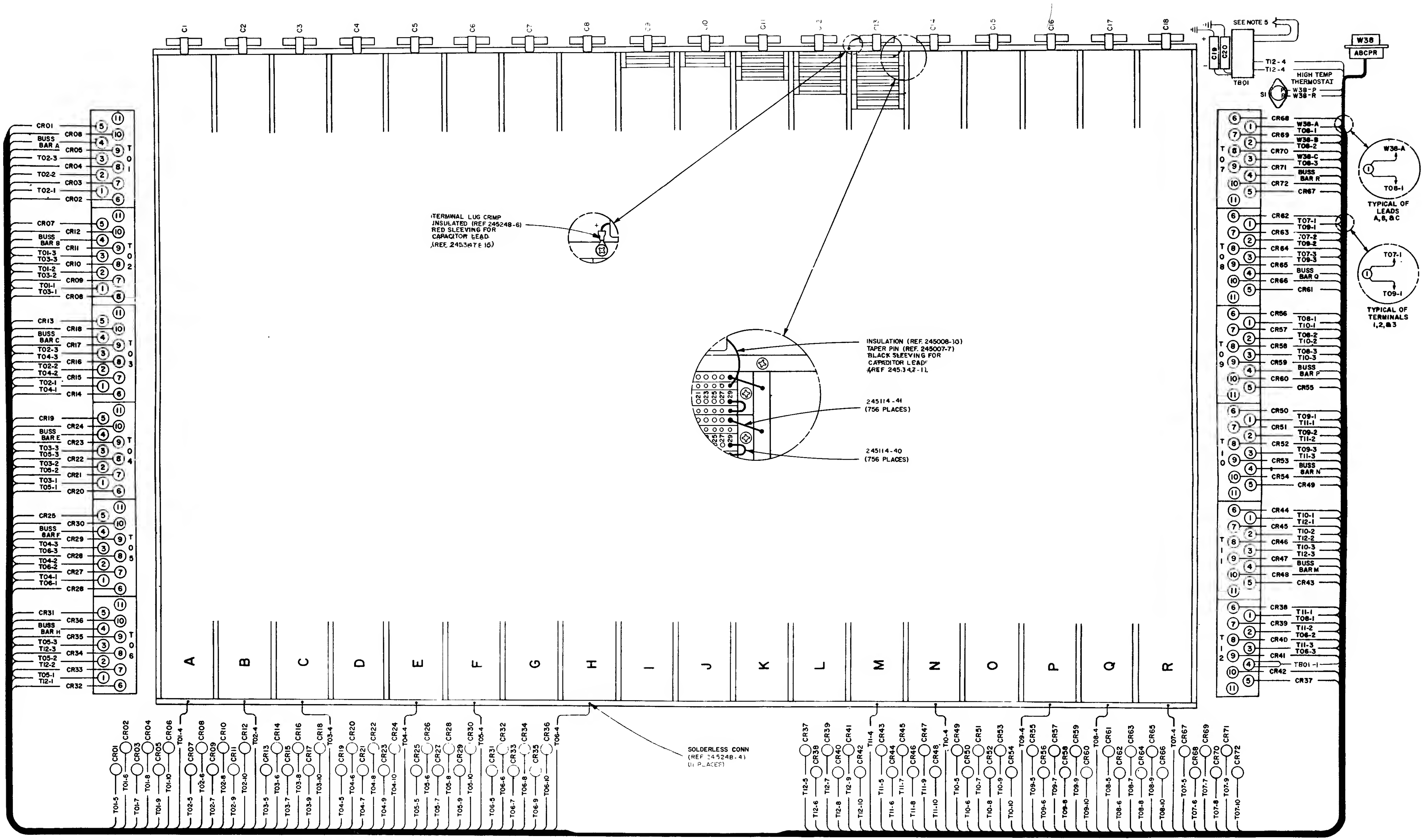
6 CAPACTORS MOUNTED WITHIN THE CIRCUIT BREAKER ARE MOUNTED WITHIN THE + LEAD SOLDERED TO PIN 1 OF THE CORRESPONDING CIRCUIT BREAKER AND THE NEGATIVE LEAD IS FASTENED TO AN ADJACENT MOUNTING SCREW BY A SOLDER LUG, (REF 8177) OR EQUIV. THE CAPACITOR LEADS ARE COVERED WITH TUBING AS SPECIFIED FOR THE BUSS-BAR CAPACITORS

7 -20V JUMPER WIRES MUST BE 18 AWG, STRD INS WIRE PER CONTROL DATA CORP. 245483-91. THE NUMBER AND LOCATION OF THE -20V JUMPERS ARE DETERMINED BY THE APPROPRIATE SYNCHRONIZER TABS.

8 USE CAPACITOR (REF 245072-37) & RECTIFIERS CR37 THRU CR42 (REF 24561601) & RECTIFIERS CR01 THRU CR36 & CR43 THRU CR72 (REF 24561602)

9 FOR WIRE LISTING SEE 63762900

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE POWER WIRING ODD MEMORY CHASSIS	PRODUCT 6601/6604/6613/6614 SIZE C · DRAWING NO 60119300 · REV BD SHEET · PAGE 15



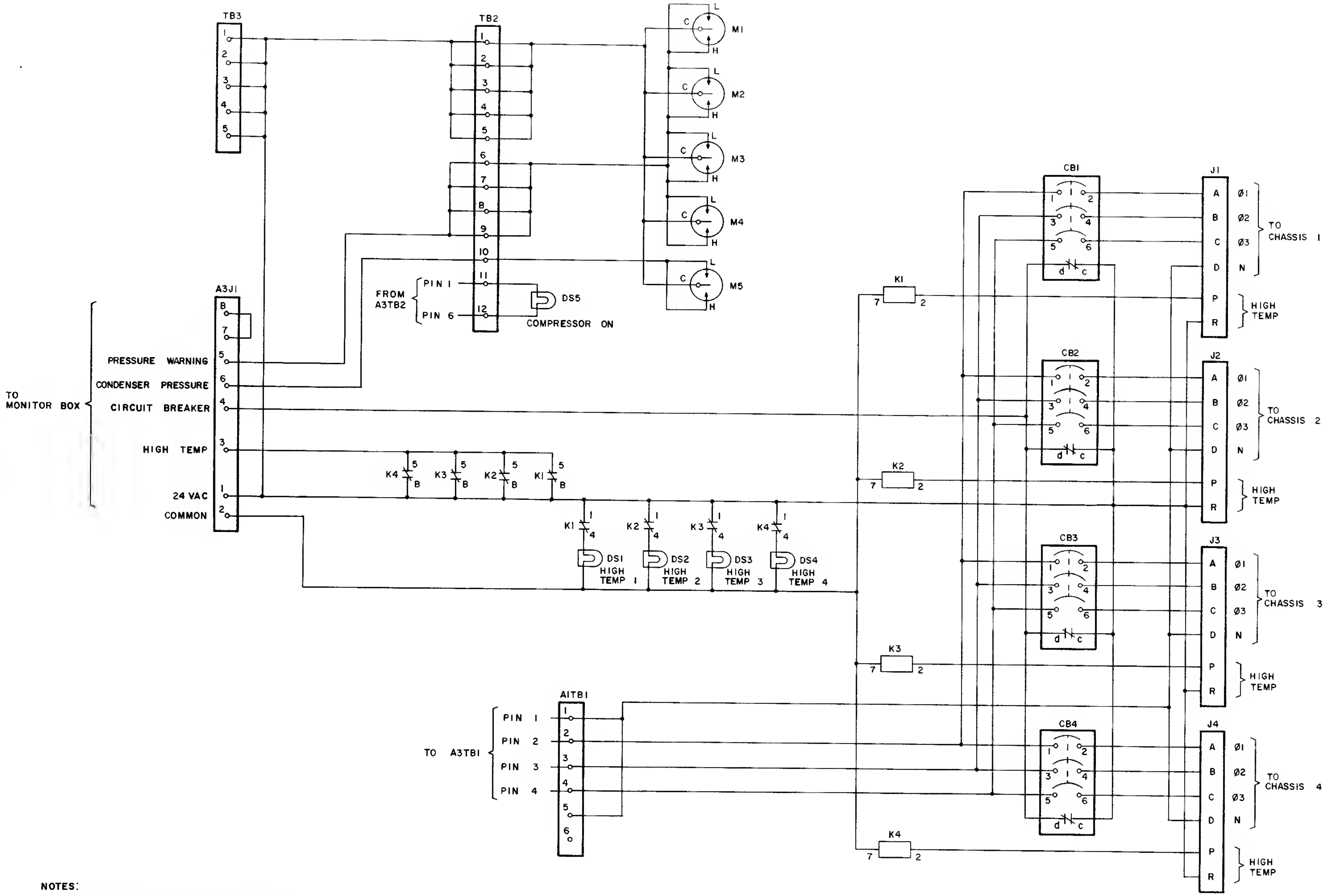
NOTES

1. FOR REMAINING COMPONENT IDENTIFICATION & DESCRIPTION SEE 63025305
2. ALL POWER-IN WIRING (W38-A, ETC.) MUST BE 18AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-87 ALL POWER WIRING TO BUSS BARS & RECTIFIERS FROM T01-T11 MUST BE 14 AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-143 POWER WIRING FROM T12-5,6,7,8,9,10. TO RECTIFIERS MUST BE 14AWG, STRD INS WIRE PER CONTROL DATA CORP 245483-147 POWER WIRES FROM T12-4 TO TAPER PINS ON -20V JUMPER WIRES MUST BE 18AWG, STRANDED INS WIRE PER CONTROL DATA CORP 245483-91
3. TRANSFORMERS T01-T11 ARE 970101 (+6V) TRANSFORMER T12 IS 100043 (-20V)
4. BUSS-BAR CAPACITOR POLARITY + TO BUSS-BAR - TO CONNECTOR
5. THE NUMBER AND LOCATION OF -20V W... DETERMINED BY THE APPROPRIATE SYNCHRO...
6. CAPACITORS ARE (REF 245072-37) & RECTIFIERS CR3... CR42 ARE REF 245616... CR43 THRU CR72 ARE REF 245...
7. FOR WIRE LISTING SEE ...

B-60119300

POWER WIRING CHASSIS 12

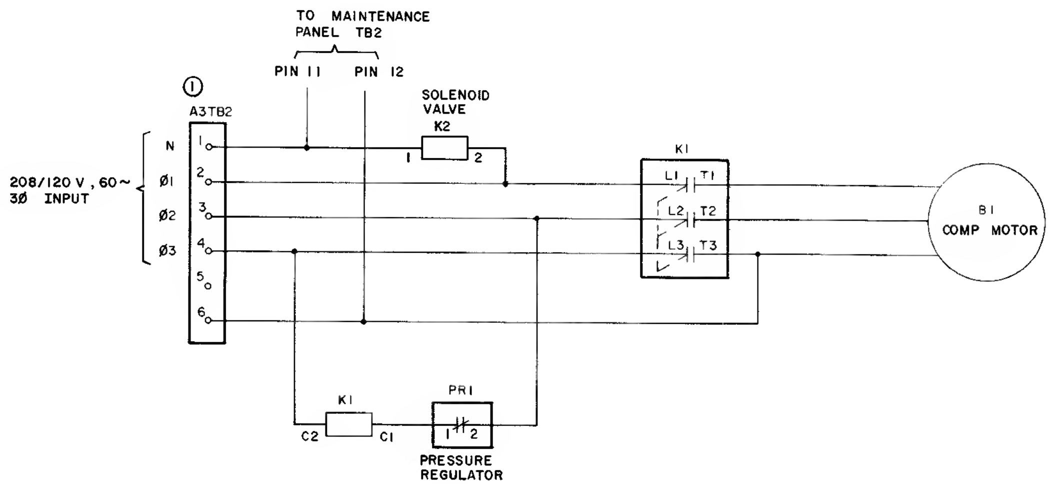
REV. K 17

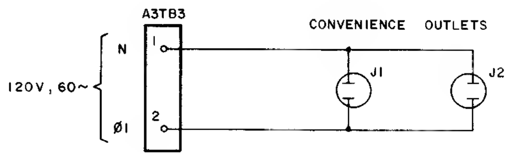


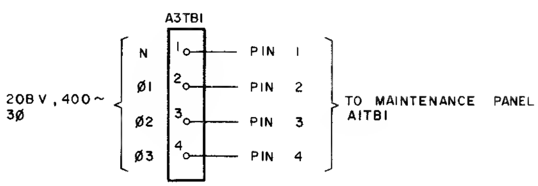
NOTES:

1. THIS CIRCUIT IS TYPICAL FOR 1 BAY.
2. BECAUSE THERE IS NO CHASSIS 11 IN BAY 3, THE RELAY K3 IN BAY 3 MAINTENANCE PANEL SHOULD BE REMOVED SO THAT A CONTINUOUS HIGH TEMPERATURE INDICATION DOES NOT OCCUR FOR CHASSIS 11

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE POWER WIRING MAINTENANCE PANEL (B MODEL)	PRODUCT 6600
		SIZE C DRAWING NO 60119300 REV
		SHEET 274 PAGE 19



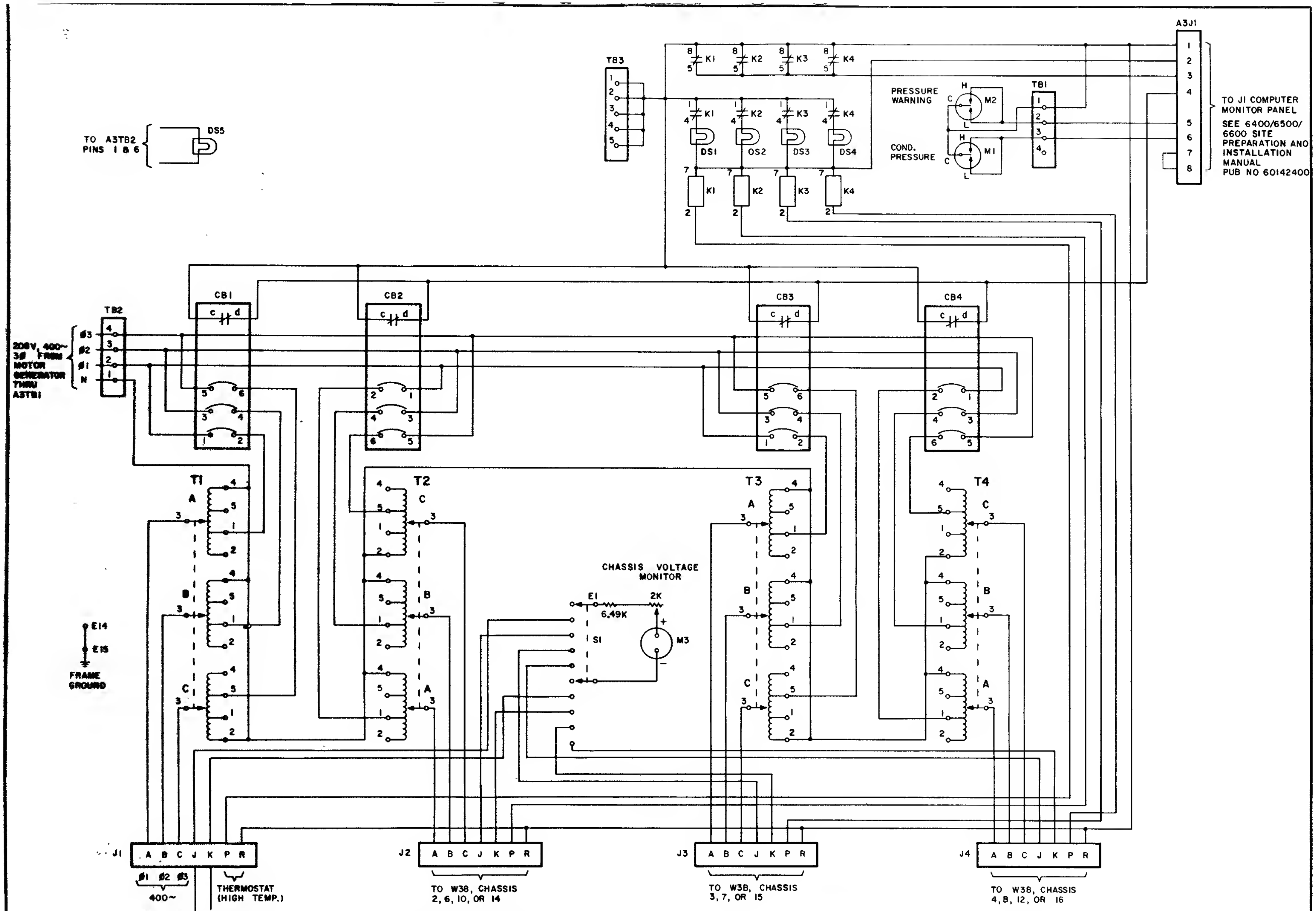




NOTE:

1. TO INSTALL A "C" SERIES CONDENSING UNIT IN PLACE OF A "B" SERIES CONDENSING UNIT, CHANGE THE WIRES NORMALLY ROUTED FROM THE CONDENSING UNIT TO A3TB3 PINS 3 & 4 (SHOWN ON PAGE 25) TO A3TB2 PINS 1 & 2, RESPECTIVELY. ALL OTHER WIRING REMAINS THE SAME AS THAT OF THE "B" SERIES CONDENSING UNIT SHOWN ON THIS PAGE.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE: CONDENSER UNIT & CABINET POWER WIRING (B MODEL)	PRODUCT 6600
		SIZE C; DRAWING NO 60119300
		SHEET 275; PAGE 21



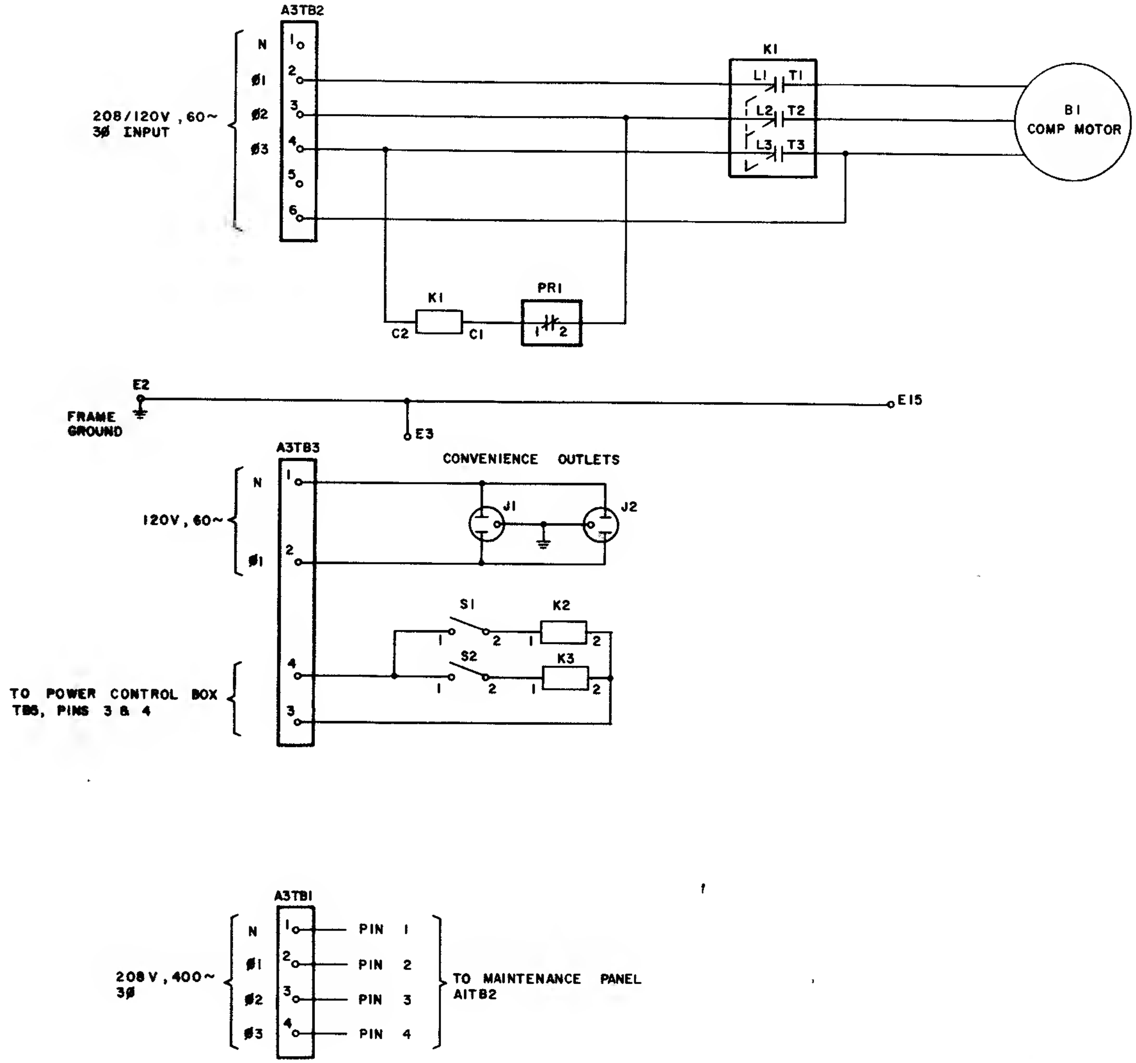
NOTES:

1. THIS CIRCUIT IS TYPICAL FOR ONE BAY.
2. PINS D, E AND F ARE SPARE WIRES FOR J1, THRU J4.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: CENTRAL COMPUTER (C MODEL) POWER WIRING COMPUTER MAINTENANCE PANEL, DRAWING 1

PRODUCT: 6600
SIZE: C
DRAWING NO: 60119300
REV: BT
SHEET: 276
PAGE: 23



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONDENSER UNIT & CABINET POWER WIRING (C MODEL)	PRODUCT 6400 SIZE C · DRAWING NO 60119300 · REV SHEET 277 · PAGE 25

PERIPHERAL and CONTROL PROCESSOR INSTRUCTIONS

INSTRUCTION TYPE	ADDRESSING MODE				
	DIRECT	INDIRECT	MEMORY	NO ADDRESS	CONSTANT
Load	30	40	50	14	20
Add	31	41	51	16	21
Subtract	32	42	52	17	
Logical Difference	33	43	53	11	23
Store	34	44	54		
Replace Add	35	45	55		
Replace Add One	36	46	56		
Replace Subtract One	37	47	57		
Long Jump			01		
Return Jump			02		
Unconditional Jump				03	
Zero Jump				04	
Non-Zero Jump				05	
Positive Jump				06	
Minus Jump				07	
Shift				10	
Logical Product				12	22
Selective Clear				13	
Load Compliment				15	

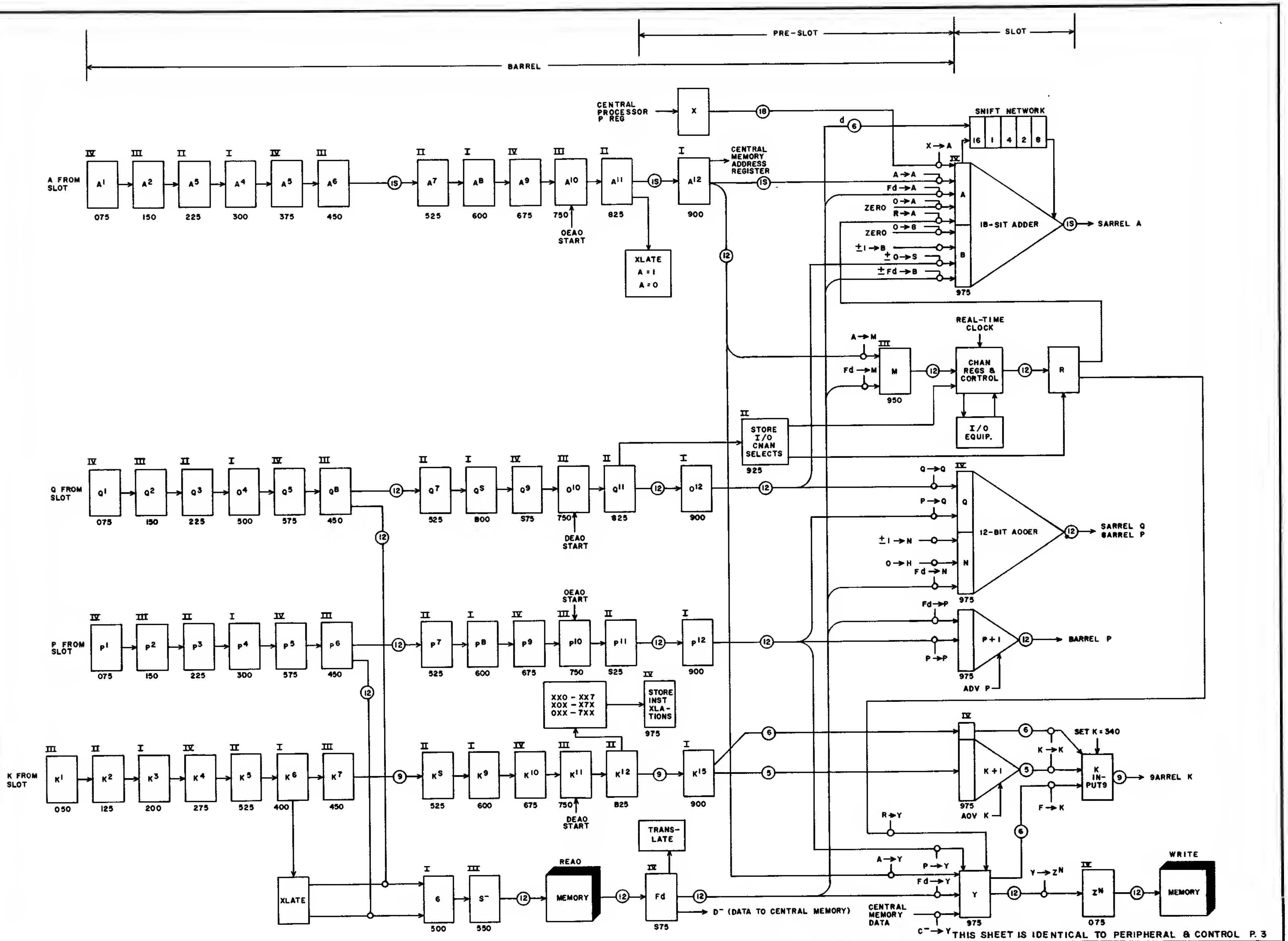
P | F | d |

- Direct Mode: d = memory address of operand   operand = (d)
- Indirect Mode: d = memory address of the address of the operand   operand = ((d))
- No Address Mode: d = operand or shift count   operand = d

P | F | d |

P + 1 | M |

- Memory Mode: d = address of the incrementer for the address of the operand   operand = ((d))+M
  M = base address of the operand (d) + M = address of operand
- Constant Mode: dM = 18 bit operand   operand - dM



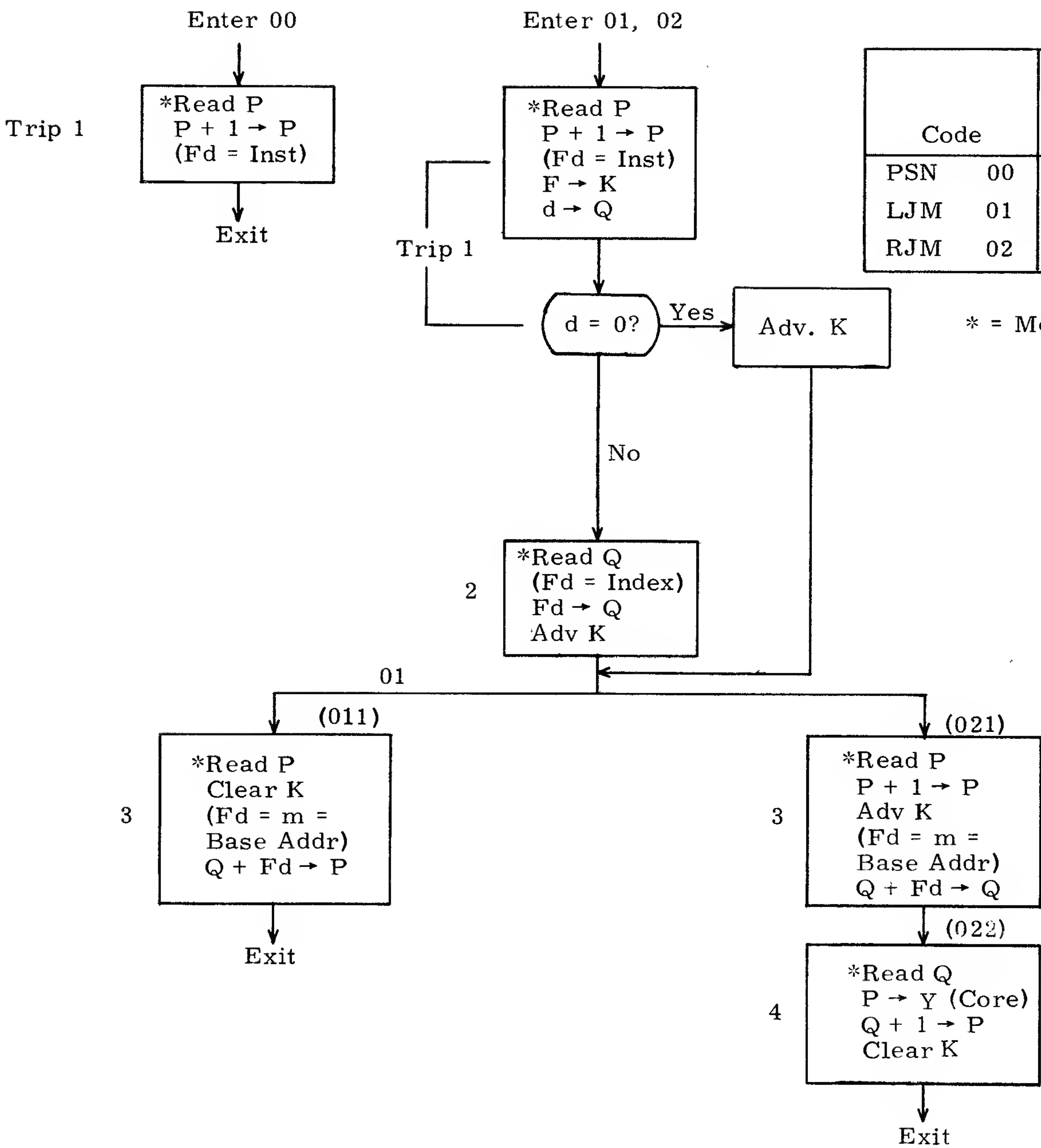
THIS SHEET IS IDENTICAL TO PERIPHERAL & CONTROL P. 3

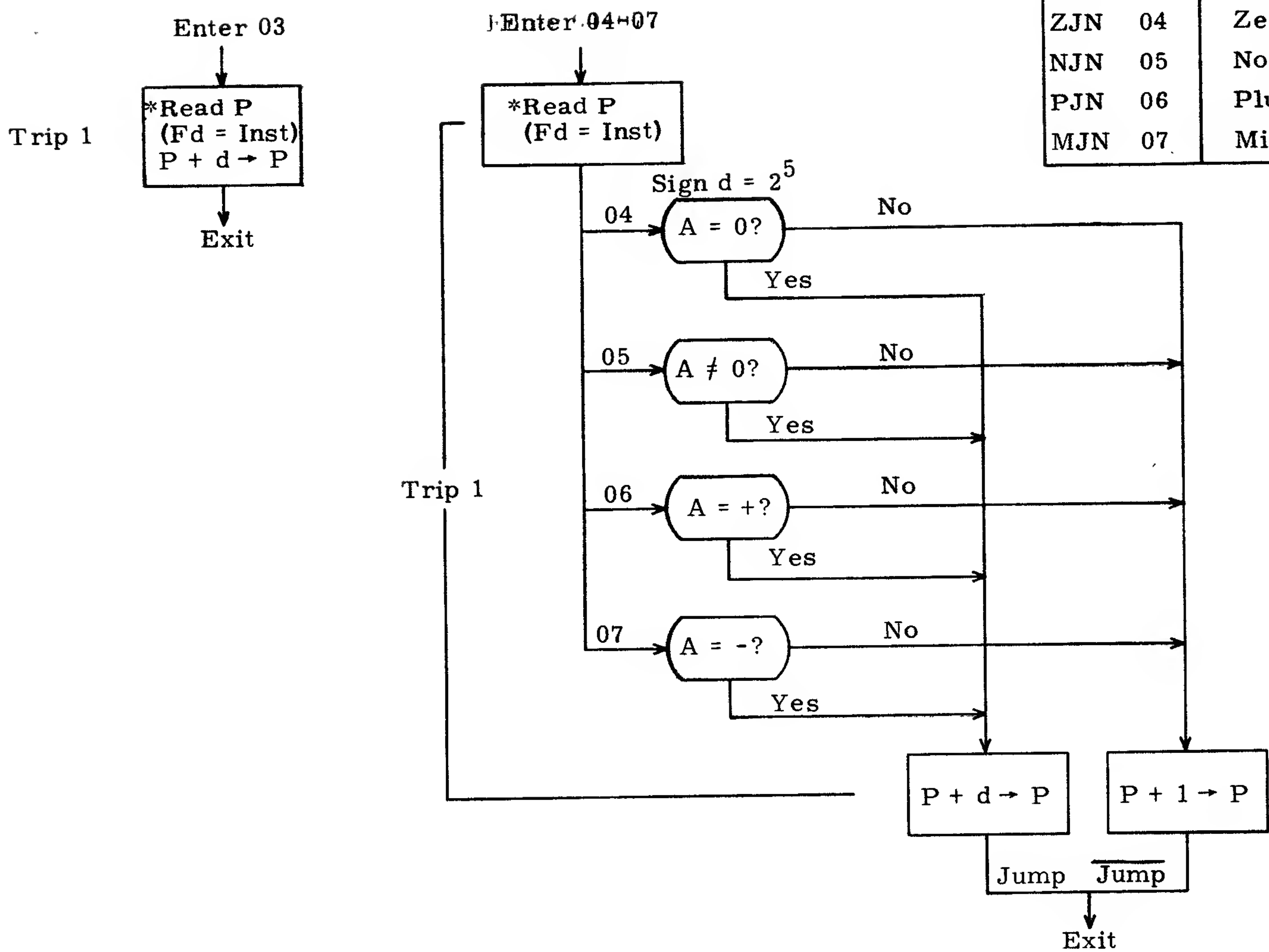
NOTE
ALL PERIPHERAL AND CONTROL PROCESSOR MODULES ON CHASSIS I

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE PERIPHERAL AND CONTROL PROCESSOR DETAIL BLOCK DIAGRAM	PRODUCT 6601/04 SIZE C — DRAWING NO. 60119300 — REV	SHEET 4 — 2

Code		Name	Time (Major Cycles)
PSN	00	Pass	1
LJM	01	Long jump to m + (d)	2-3
RJM	02	Return jump to m + (d)	3-4

* = Memory Ref



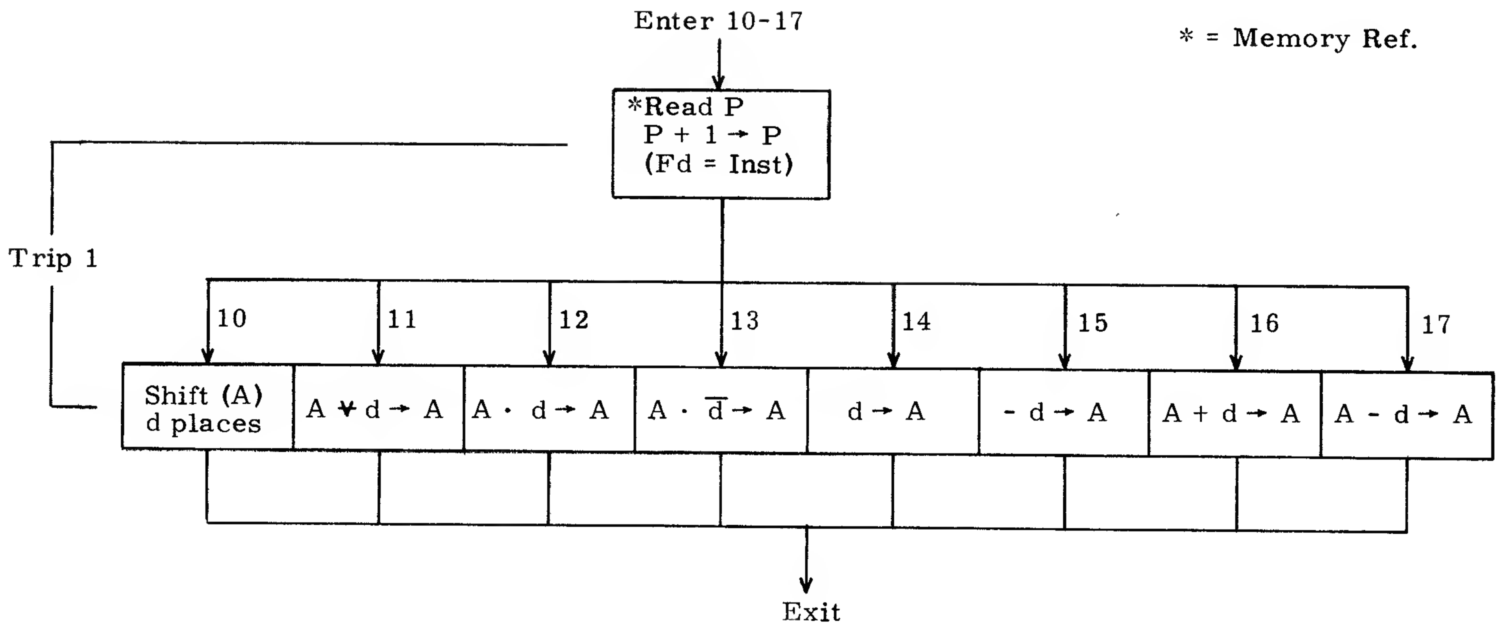


Code		Name	Time (Major Cycles)
UJN	03	Unconditional jump d	1
ZJN	04	Zero jump d	1
NJN	05	Nonzero jump d	1
PJN	06	Plus jump d	1
MJN	07	Minus jump d	1

* = Memory Ref

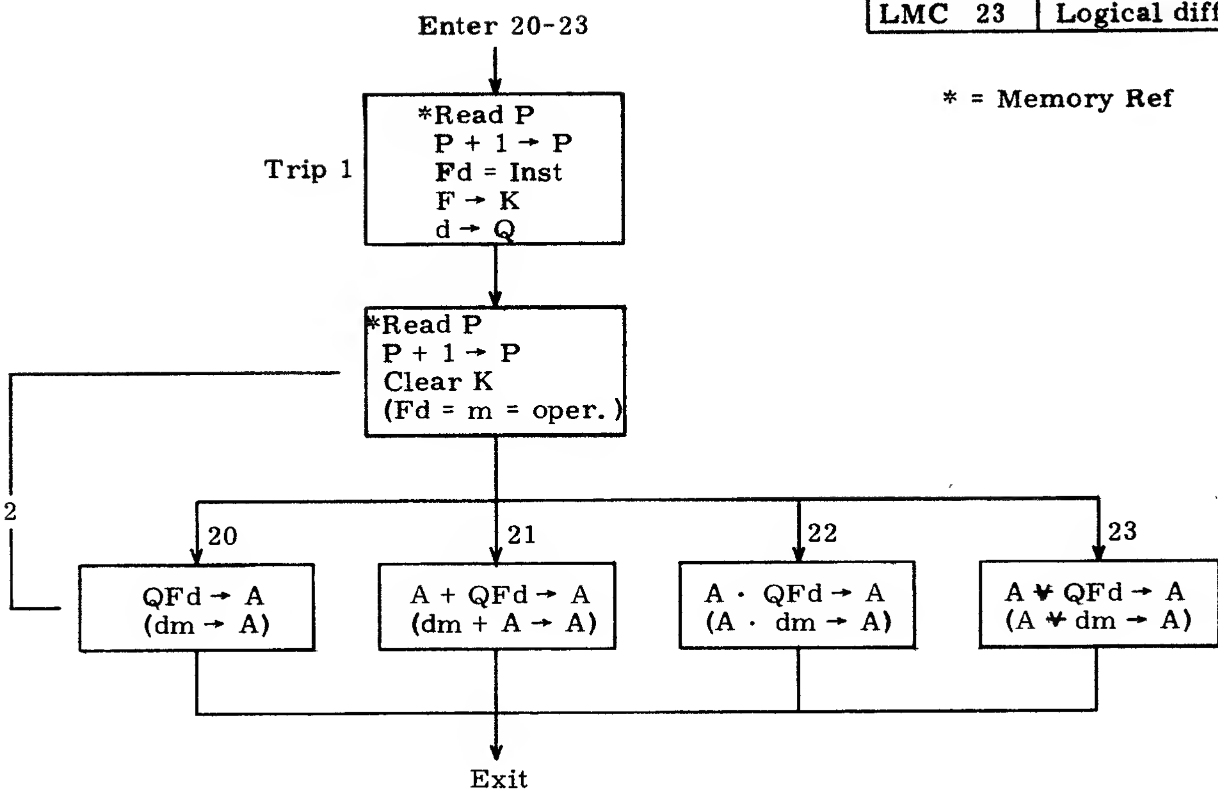
Code		Name	Time (Major Cycles)
SHN	10	Shift d	1
LMN	11	Logical difference d	1
LPN	12	Logical product d	1
SCN	13	Selective clear d	1
LDN	14	Load d	1
LCN	15	Load complement d	1
ADN	16	Add d	1
SBN	17	Subtract d	1

* = Memory Ref.



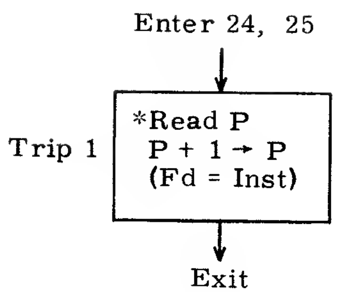
Code		Name	Time (Major Cycles)
LDC	20	Load dm	2
ADC	21	Add dm	2
LPC	22	Logical product dm	2
LMC	23	Logical difference dm	2

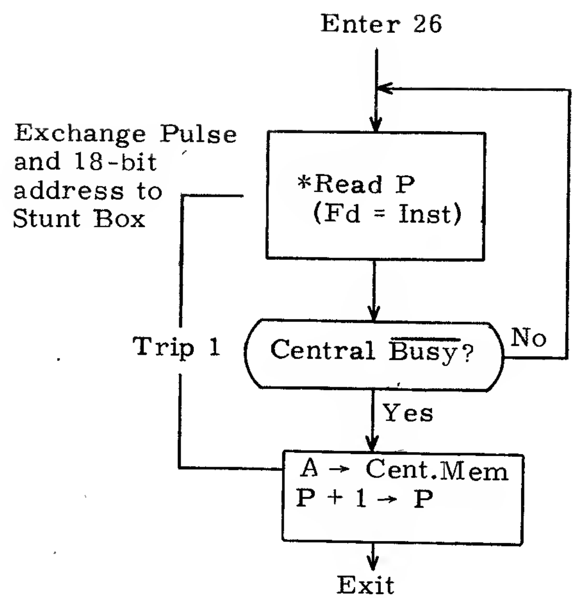
* = Memory Ref

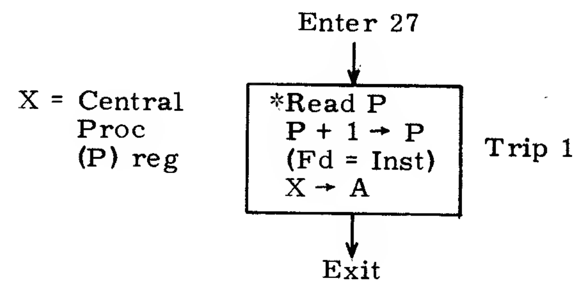


Code		Name	Time (Major Cycles)
PSN	24	Pass	1
PSN	25	Pass	1
EXN	26	Exchange jump	min. 2.0
RPN	27	Read program address	1

* = Memory Ref.

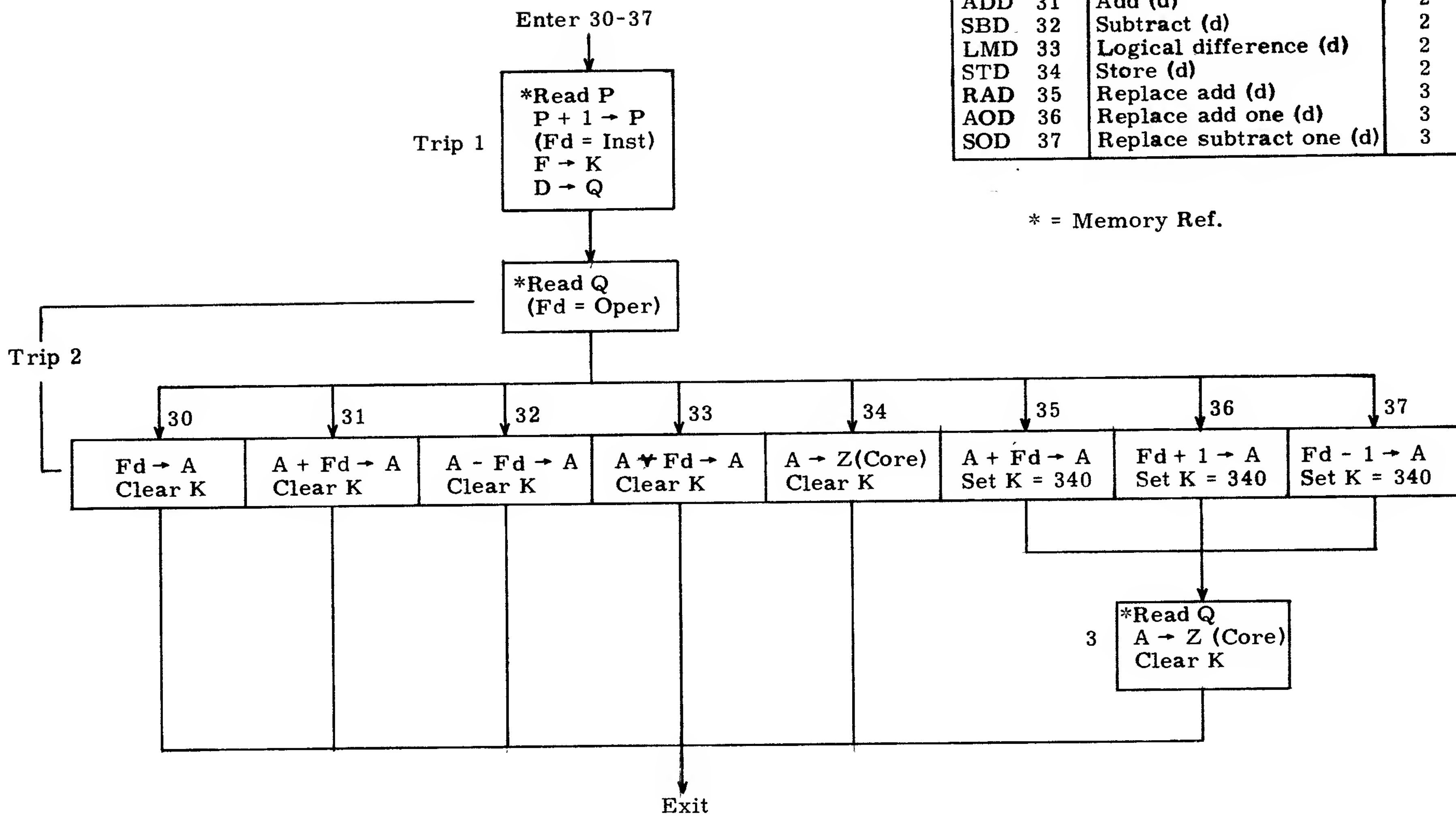


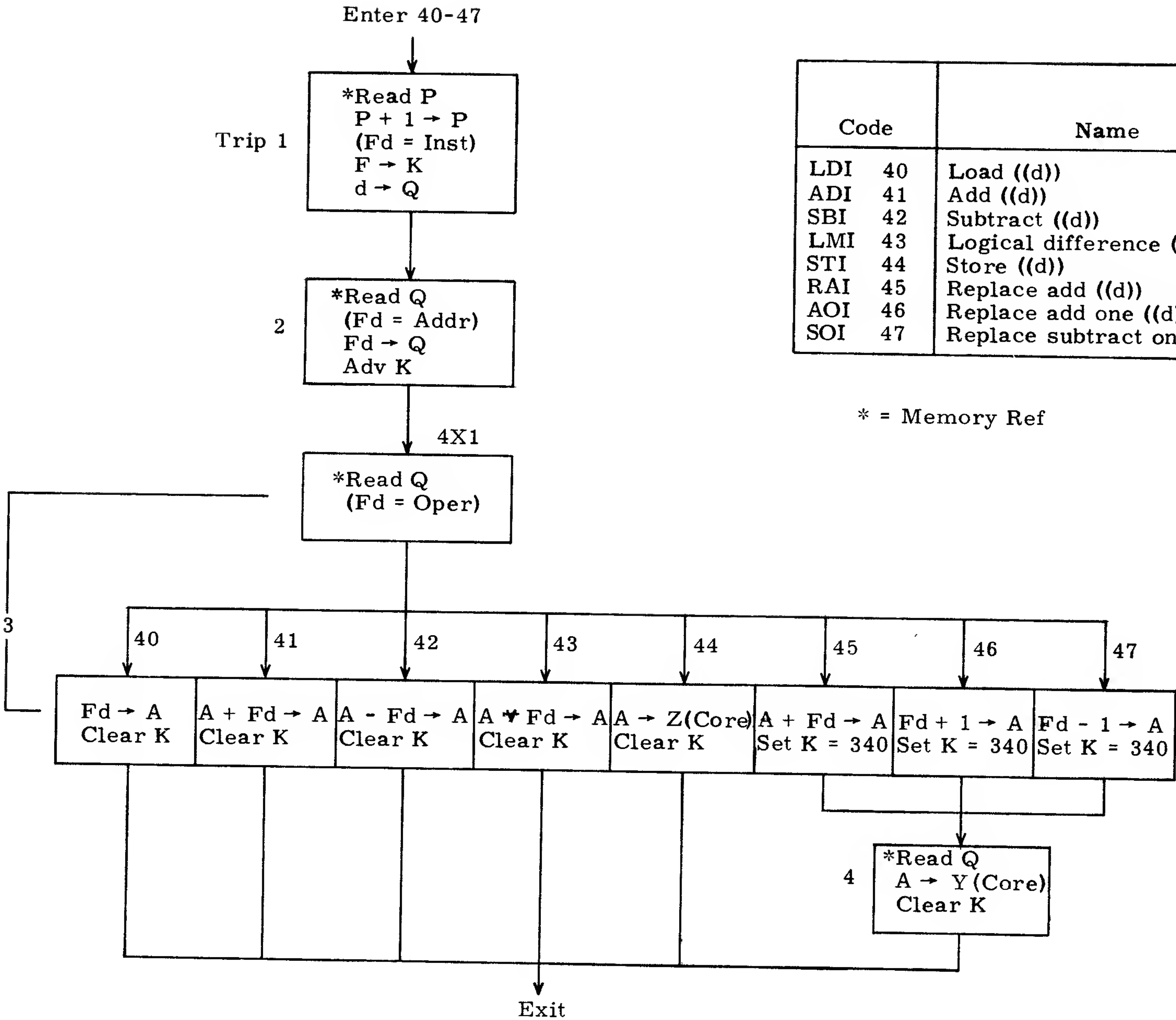




Code		Name	Time (Major Cycles)
LDD	30	Load (d)	2
ADD	31	Add (d)	2
SBD	32	Subtract (d)	2
LMD	33	Logical difference (d)	2
STD	34	Store (d)	2
RAD	35	Replace add (d)	3
AOD	36	Replace add one (d)	3
SOD	37	Replace subtract one (d)	3

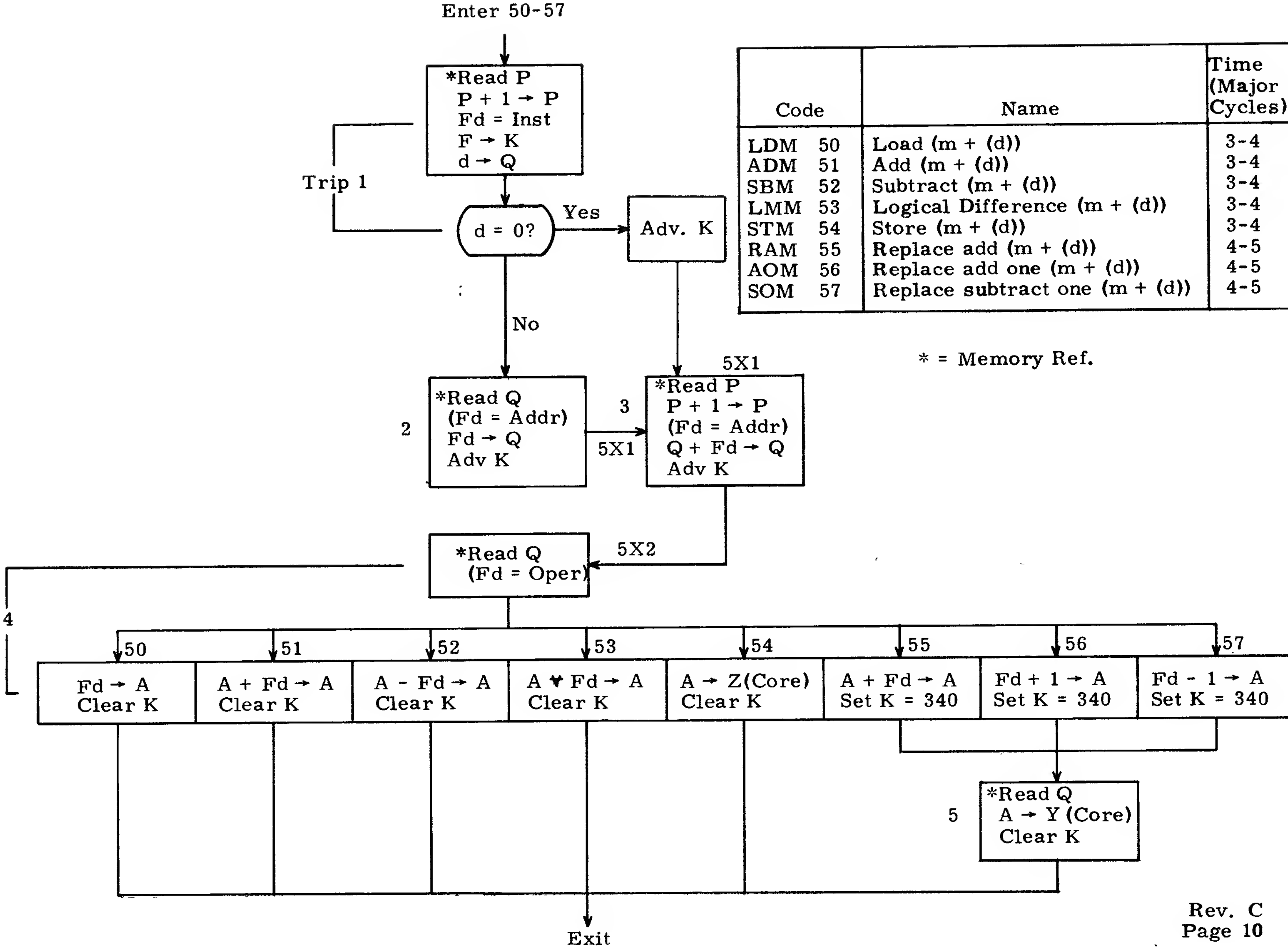
* = Memory Ref.





Code		Name	Time (Major Cycles)
LDI	40	Load ((d))	3
ADI	41	Add ((d))	3
SBI	42	Subtract ((d))	3
LMI	43	Logical difference ((d))	3
STI	44	Store ((d))	3
RAI	45	Replace add ((d))	4
AOI	46	Replace add one ((d))	4
SOI	47	Replace subtract one ((d))	4

* = Memory Ref

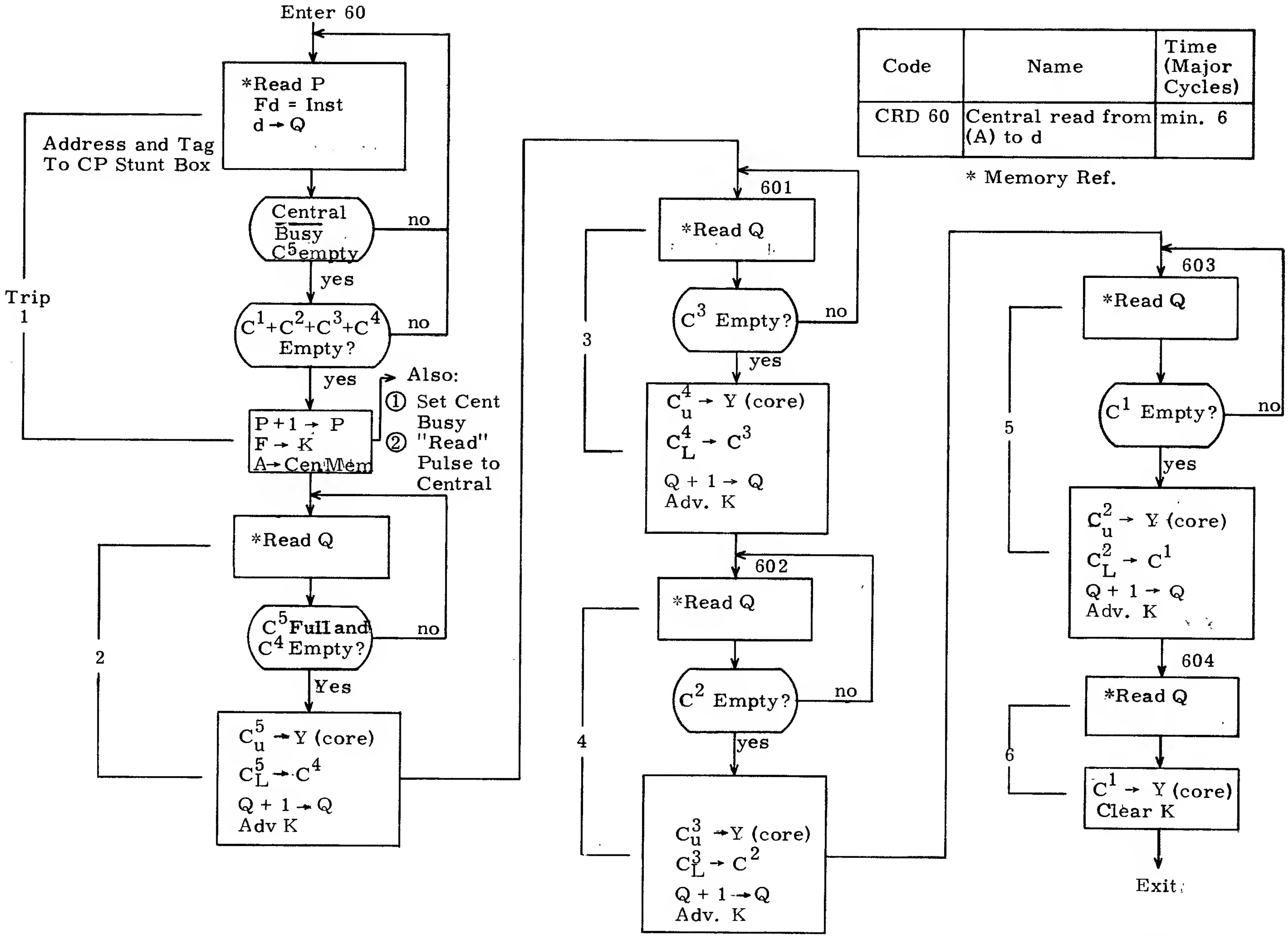


Code		Name	Time (Major Cycles)
LDM	50	Load (m + (d))	3-4
ADM	51	Add (m + (d))	3-4
SBM	52	Subtract (m + (d))	3-4
LMM	53	Logical Difference (m + (d))	3-4
STM	54	Store (m + (d))	3-4
RAM	55	Replace add (m + (d))	4-5
AOM	56	Replace add one (m + (d))	4-5
SOM	57	Replace subtract one (m + (d))	4-5

* = Memory Ref.

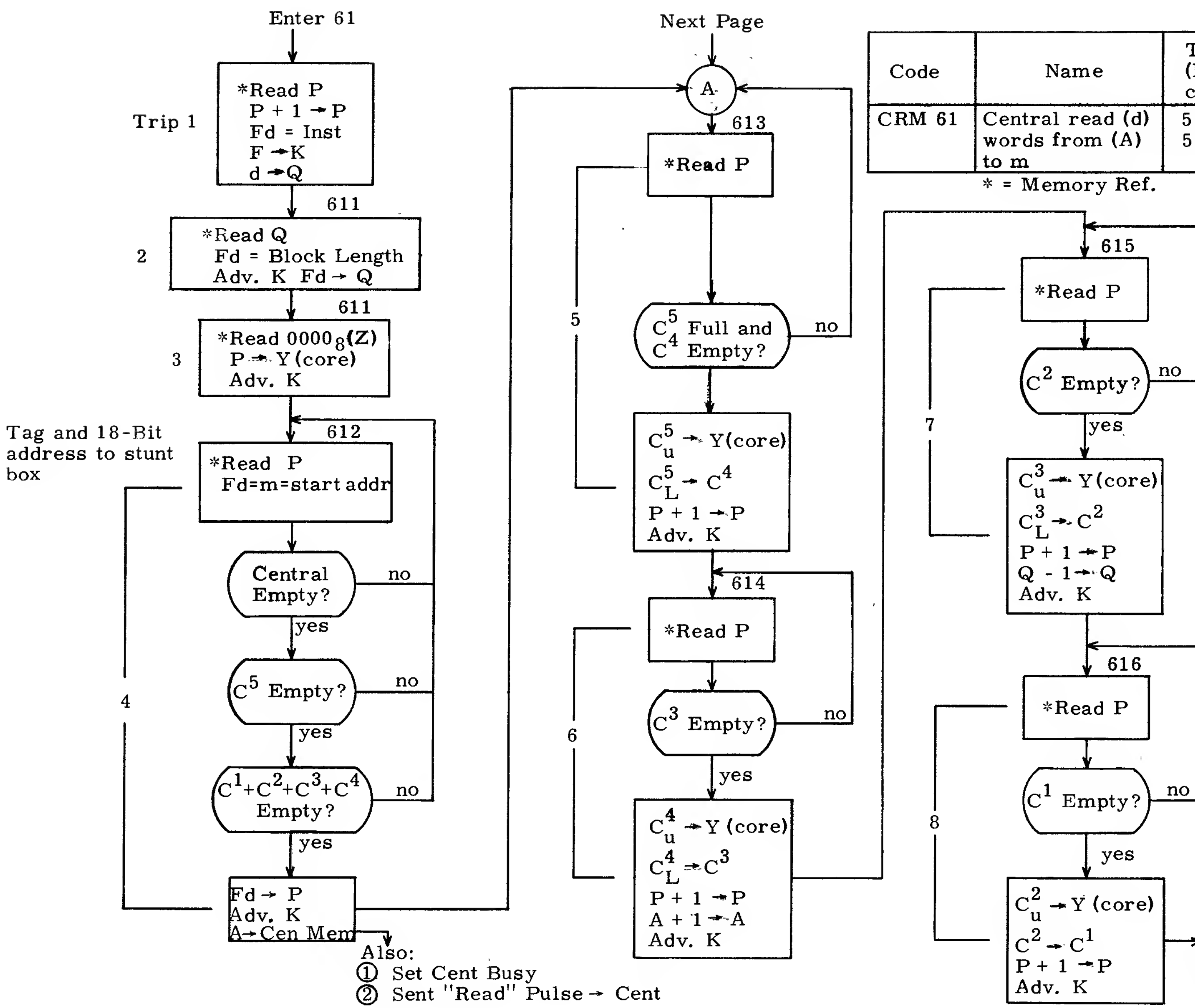
Code	Name	Time (Major Cycles)
CRD 60	Central read from (A) to d	min. 6

* Memory Ref.

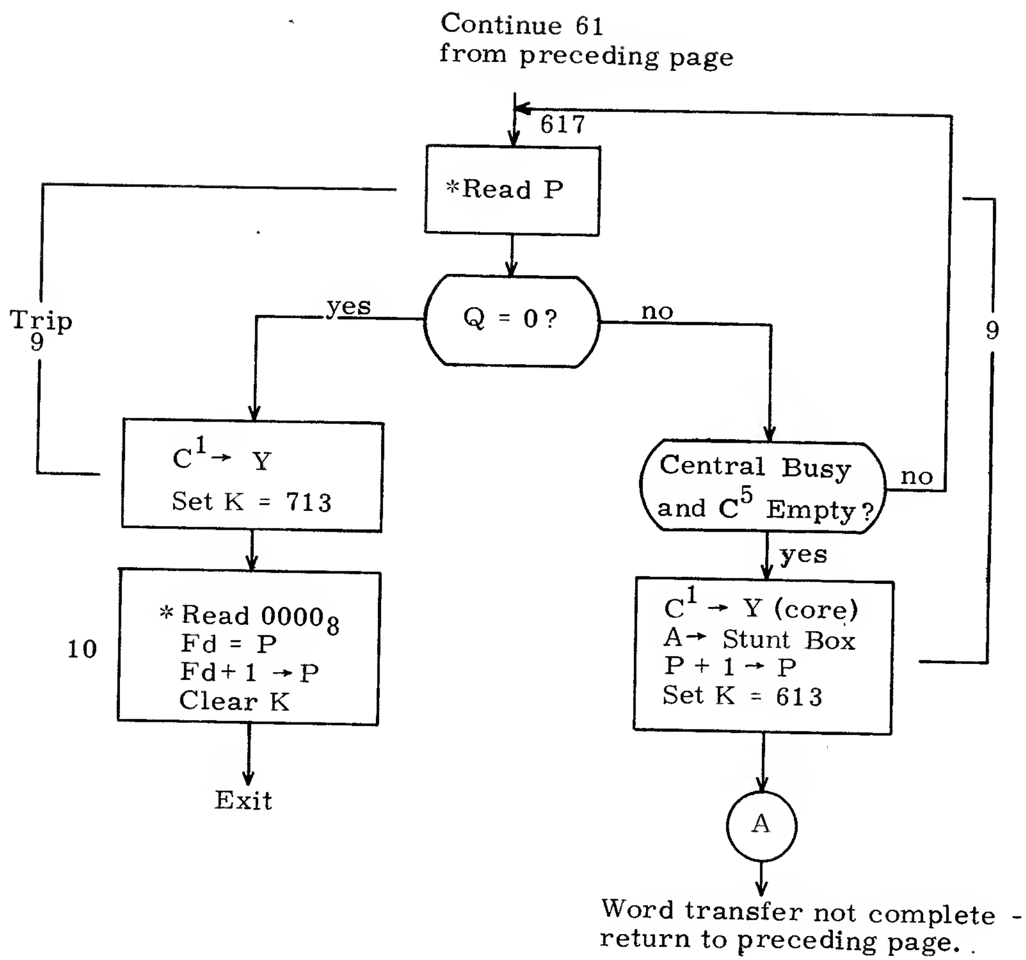


Code	Name	Time (Major cycles)
CRM 61	Central read (d) words from (A) to m	5 plus 5/word

* = Memory Ref.

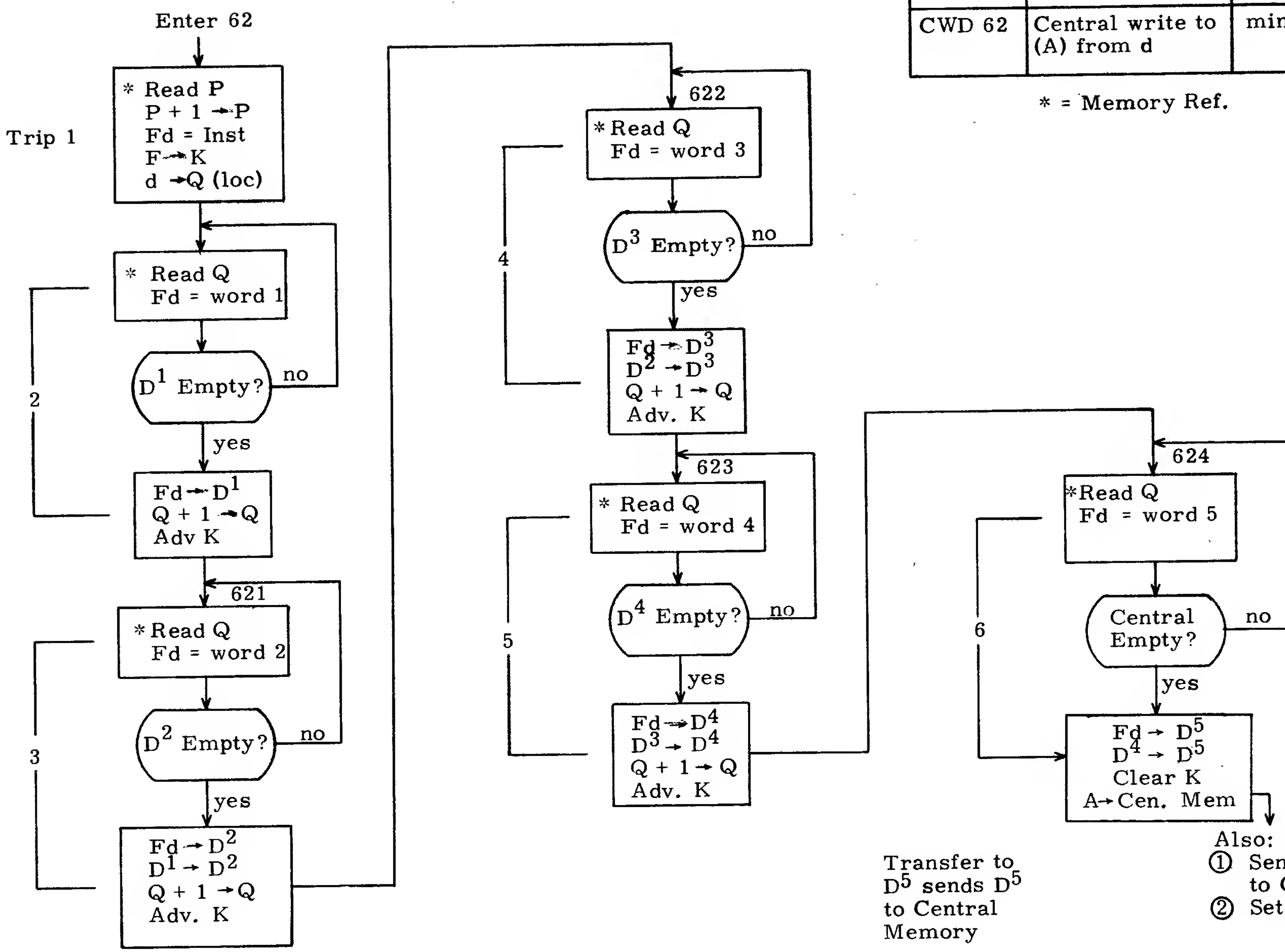


Continued on next page


Continue 61
from preceding page
617
*Read P
Q = 0 ?
yes
no
Trip
9
$C^1 \rightarrow$ Y
Set K = 713
10
* Read 0000_8
Fd = P
Fd+ 1 → P
Clear K
Exit
Central Busy
and C^5 Empty ?
no
yes
9
$C^1 \rightarrow$ Y (core)
A → Stunt Box
P + 1 → P
Set K = 613
A
Word transfer not complete -
return to preceding page.

Code	Name	Time (Major Cycles)
CWD 62	Central write to (A) from d	min 6

* = Memory Ref.



Transfer to D^5 sends D^5 to Central Memory

Also:
① Send "Write" to Central
② Set Cent Busy

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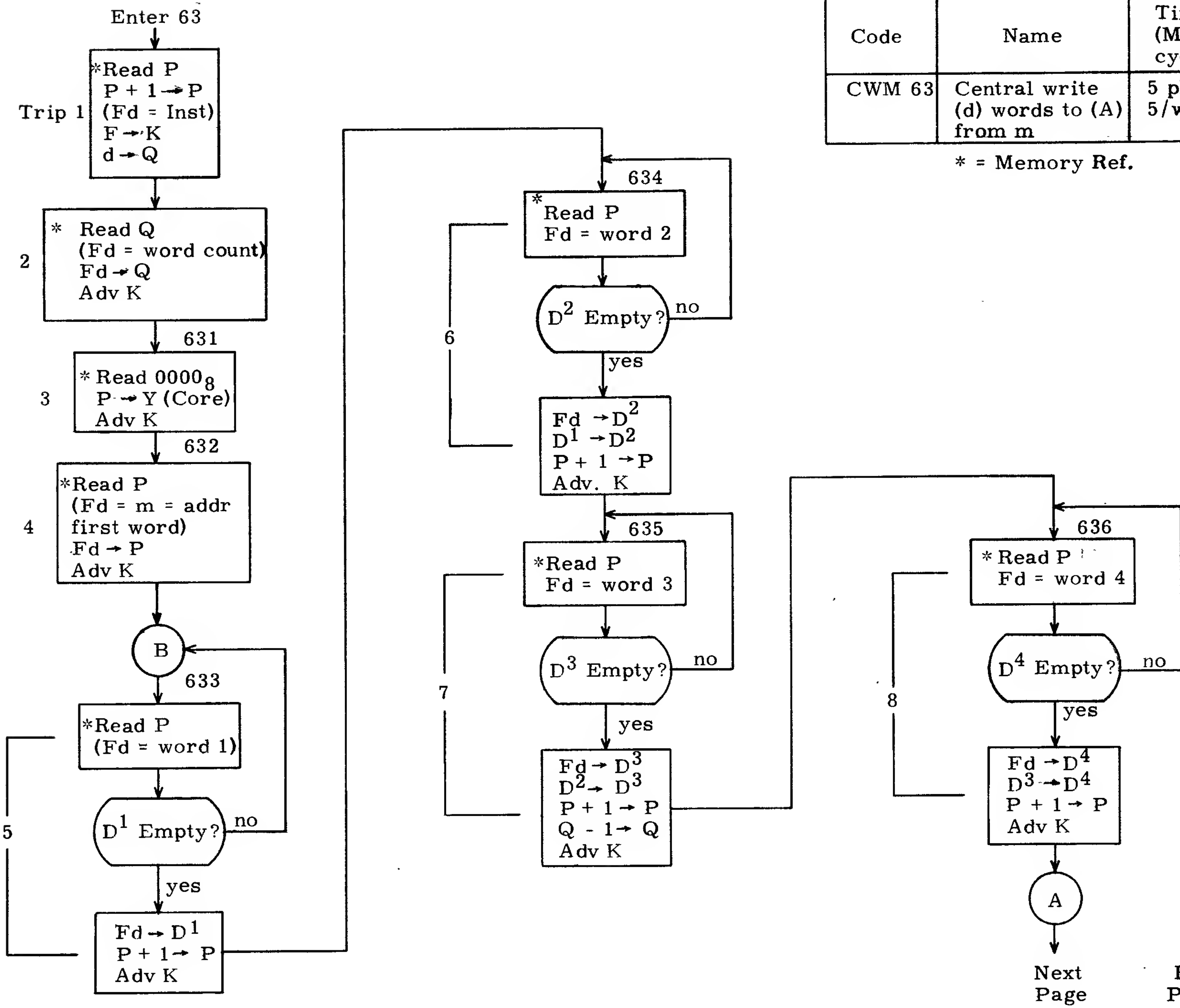
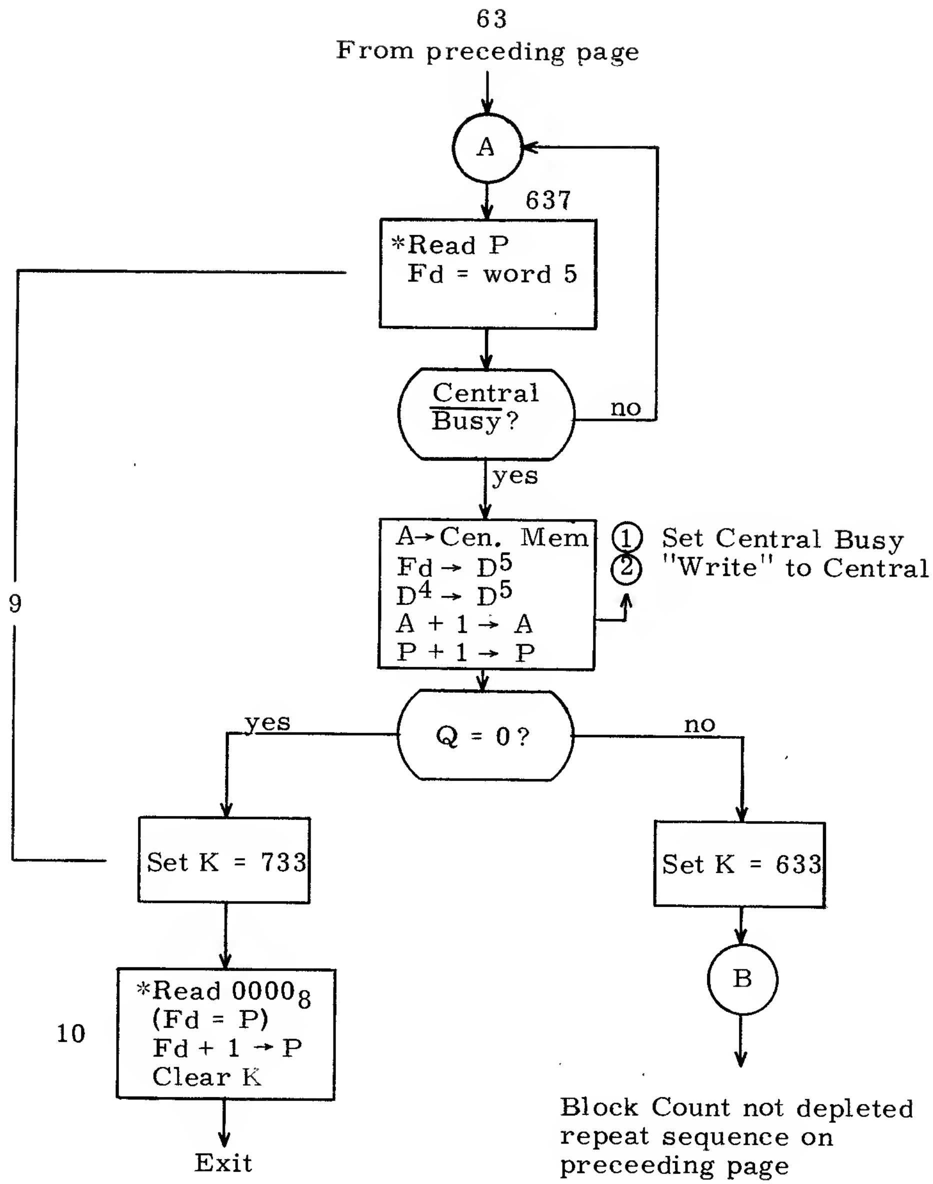
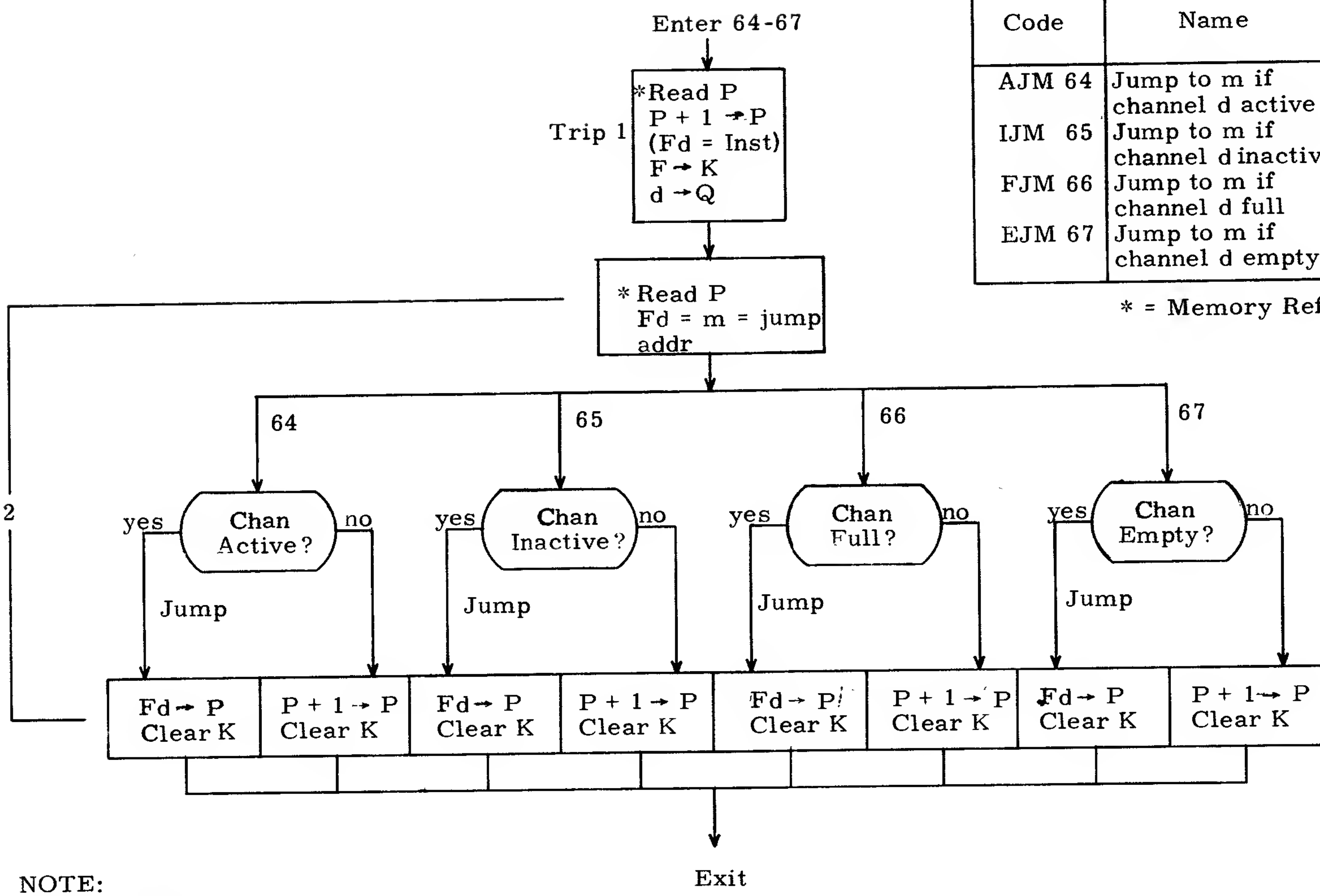
Code	Name	Time (Major cycles)
CWM 63	Central write (d) words to (A) from m	5 plus 5/word

* = Memory Ref.




63
From preceding page
A
637
*Read P
Fd = word 5
Central Busy?
no
yes
A → Cen. Mem
Fd → D^5
D^4 → D^5
A + 1 → A
P + 1 → P
1 Set Central Busy
2 "Write" to Central
9
Q = 0?
yes
no
Set K = 733
Set K = 633
B
10
*Read 0000_8
(Fd = P)
Fd + 1 → P
Clear K
Exit
Block Count not depleted
repeat sequence on
preceeding page



Code	Name	Time (Major Cycles)
AJM 64	Jump to m if channel d active	2
IJM 65	Jump to m if channel d inactive	2
FJM 66	Jump to m if channel d full	2
EJM 67	Jump to m if channel d empty	2

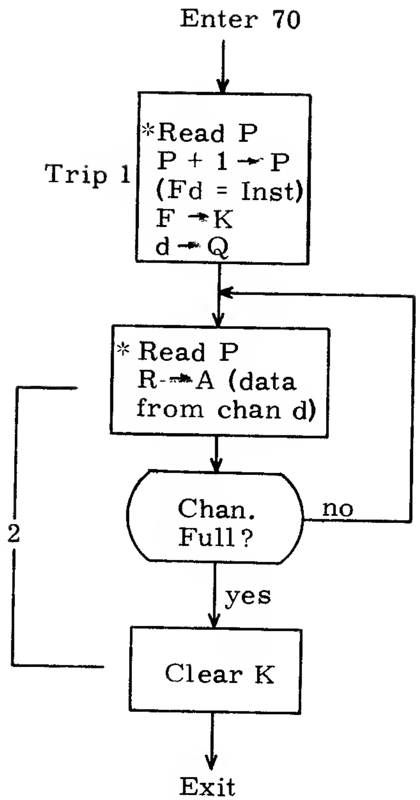
* = Memory Ref.

NOTE:

FD → P ➜ (1) Fd → H
(2) $\overline{Q \rightarrow Q}$ (Clears Q)
(3) Q Adder → P

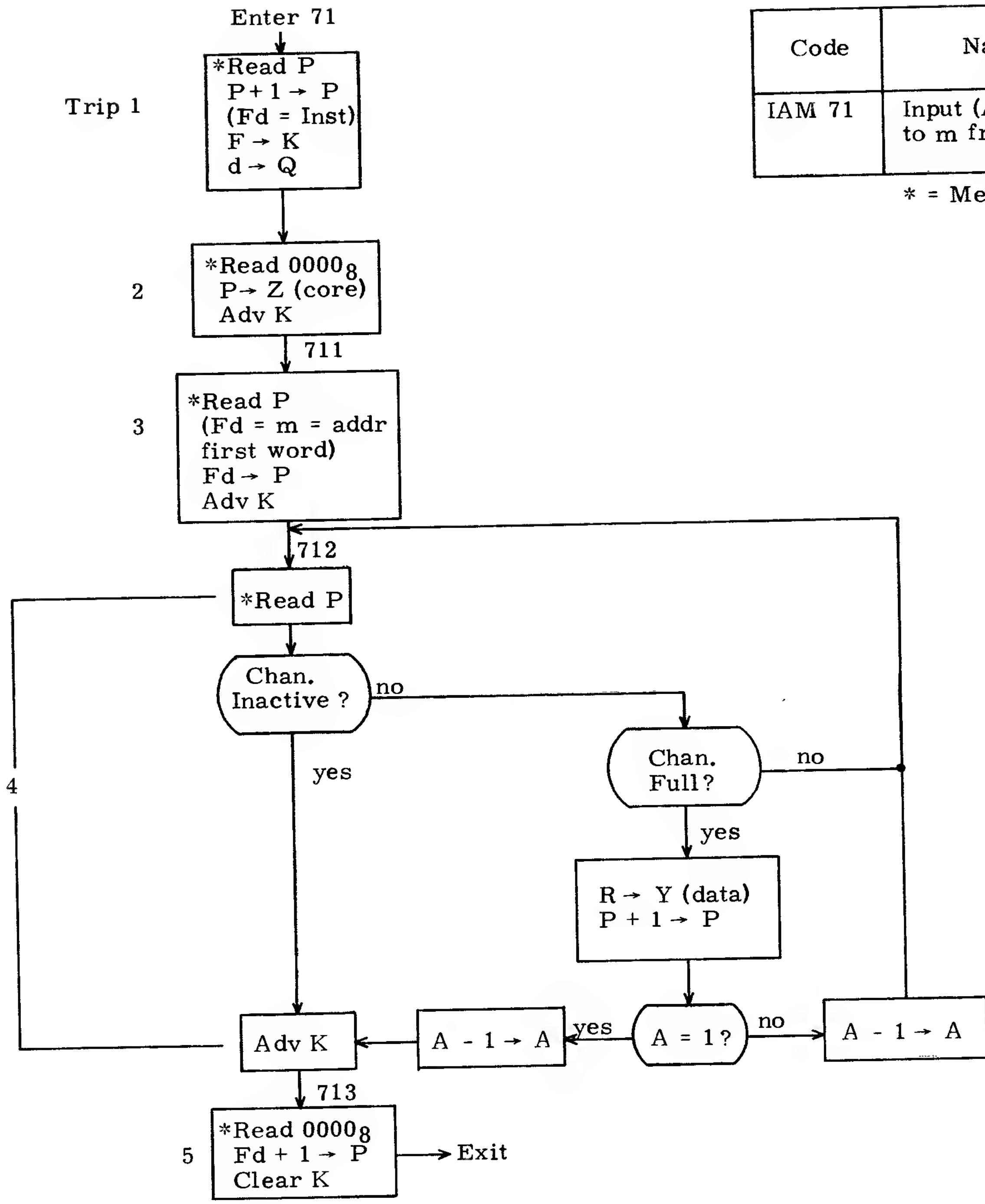
Code	Name	Time (Major Cycles)
IAN 70	Input to A from channel d	2

* = Memory Ref



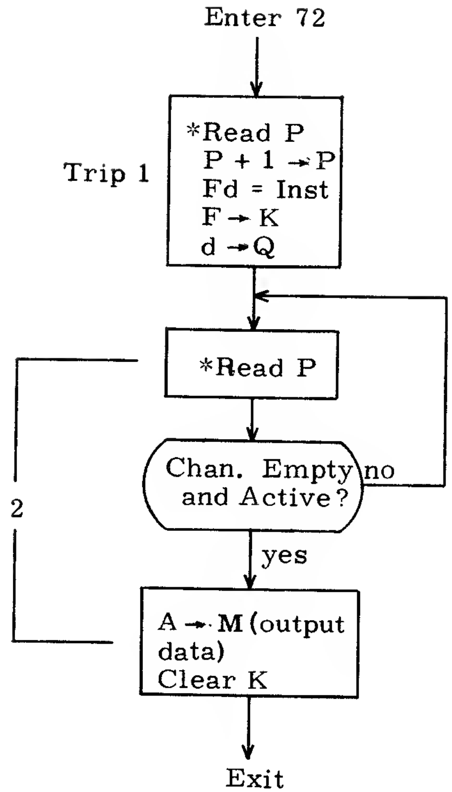
Code	Name	Time (Major cycles)
IAM 71	Input (A) words to m from chan d	4 plus 1/word

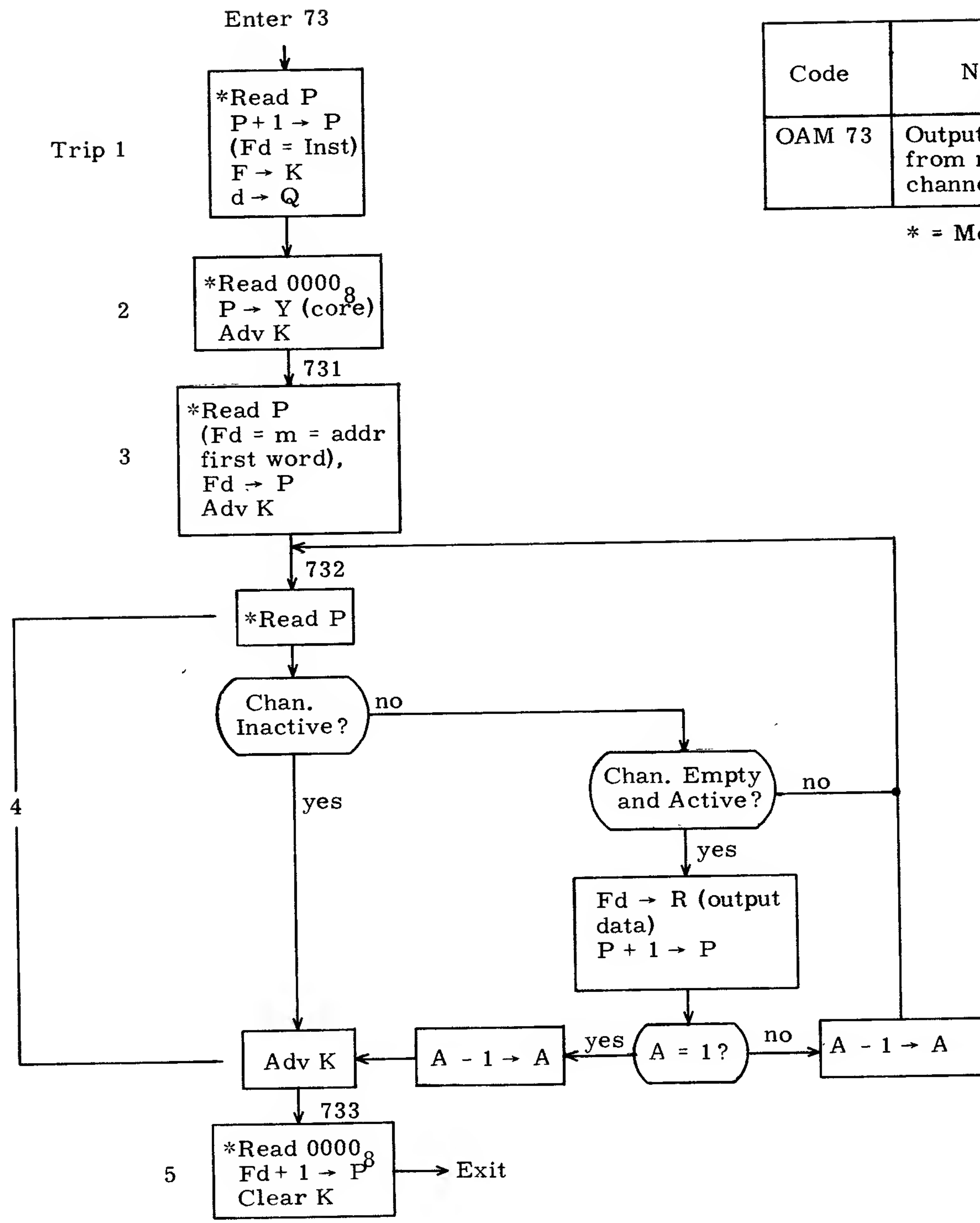
* = Memory Ref.



Code	Name	Time (Major Cycles)
OAN 72	Output from A on channel d	2

*Memory Ref.



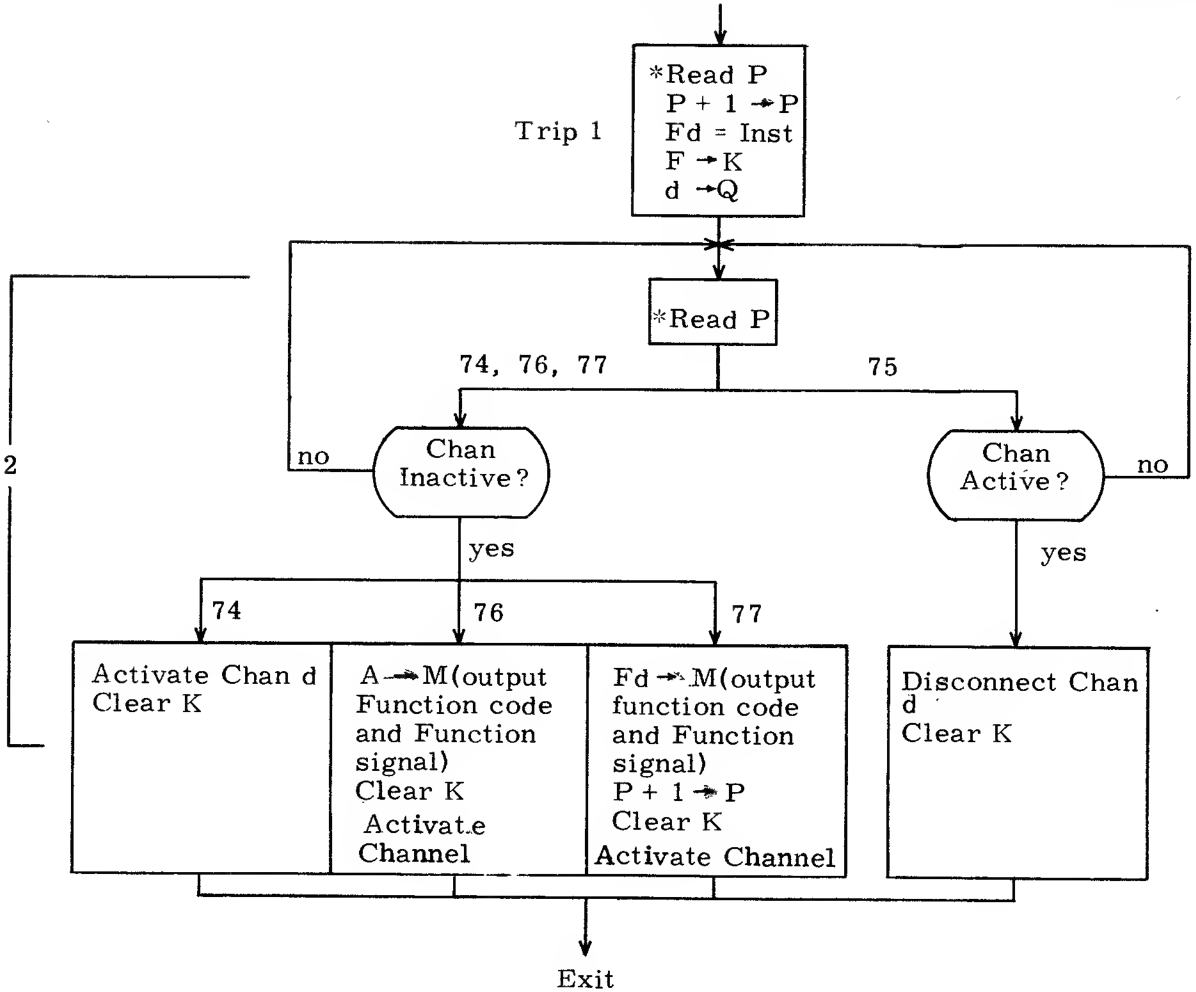


Code	Name	Time (Major cycles)
OAM 73	Output (A) words from m on channel d	4 plus 1/word

* = Memory Ref.

Code	Name	Time (Major cycles)
ACN 74	Activate channel d	2
DCN 75	Disconnect channel d	2
FAN 76	Function (A) on channel d	2
FNC 77	Function m on channel d	2

* = Memory Ref



APPENDIX A

6601 CENTRAL COMPUTER
PERIPHERAL and CONTROL PROCESSORS

INSTRUCTION FLOW CHARTS

Pub. No. 60119300
Rev. K

COMMENT SHEET

CONTROL DATA 6601/6604/6613/6614 CENTRAL COMPUTER

C. E. Diagrams and Circuit Description Manual, Vol. 2

Pub. No. 60119300

FROM: NAME: ____________________

BUSINESS ADDRESS: ____________________

THESE COMMENTS REFER TO REV. ______ OF THIS MANUAL.

COMMENTS: (DESCRIBE ERRORS, SUGGESTED ADDITIONS OR DELETIONS, ETC. INCLUDE PAGE NUMBER.)

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